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Harmonic Analysis and Comparison of Cascaded Inverters

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Abstract

Multilevel inverters allow a higher count of voltage levels with lower harmonics and without transformers or synchronized switching devices connected in series. This work analyzes the harmonics and total harmonic distortion on multilevel inverters. In this study, the multilevel arrangement uses a CHB inverter. III, V, VII, IX, XI and XIII level CHB inverter output harmonics and THD are investigated and compared with the help of MATLAB simulation. And output voltage is being analyzed using the Fourier series. It is found that the total harmonics distortion and harmonics are suppressed using higher levels of CHB multilevel inverter architectures.

Keywords—Multilevel Inverter (MLI), Total Harmonic Distortion (THD), Cascaded, Harmonics, Cascaded H Bridge (CHB).

I. INTRODUCTION

A multi-level inverter (MLI) is a power electronic converter that uses electronic control. A MLI, work's with more than two levels of voltage to produce an output voltage waveform that is smooth and stepped (Al-Hitmi et al., 2022). The output voltage from more than two levels has a lower ratio and fewer harmonic distortions (T. Roy et al., 2021) . The smoothness of the output voltage increases according to the voltage levels, and the output waveform gets more smooth as the voltage levels rise (A. Akbari et al., 2022) (S. T. Meraj et al., 2022). There are several multi-level inverter topologies available. The input voltage from the source to MLI and how switches operate differ. "Akagi, Takashi, and Nabae" first proposed diode clamped Inverter, which was known as a neutral point converter. The diode-clamped multilevel inverters employ clamping diodes to limit the voltage stress on the components (S. Ahmadi et al., 2021). A (n-1) input voltage source, (n-1)*(n-2) operational diodes, and (2n-2) switching devices are needed for a n-level inverter. Capacitor Clamped/ Flying Capacitor inverter's setup structure is similar to the one in the one before it, with the exception of capacitors being employed to restrict voltage instead of diodes (R. Sun et al., 2022). In order to restrict voltage, a level Capacitor Clamped inverter comprises of (2n-2) switches and (n-1)*(n-2)/2 Capacitor Clamped (Z. Xu et al., 2020). Cascaded H bridge inverter works on

the principle of cascading H bridge inverters with the aim of achieving output voltage in the form of a sinusoidal waveform. The voltage produced by all cells is summed to form the output voltage (G. Zhang et al., 2021). Its output consists of 2n + 1 levels, where n is the number of cells. Also, for this configuration, the number of switches is 4n and the number of capacitors is equal to n. The chosen switches are optimum in terms of Total Harmonic Distortion (THD). This design approach requires fewer components when compared to flying capacitors or diode clamped Modular Multilevel Inverter (MLI), resulting in lighter and more cost-effective solutions. In response to the reduction of renewable energy fossil resources, new methods of generating electricity from renewable sources like photovoltaic (PV) arrays and wind turbines are being developed (M. A. Hosseinzadeh et al., 2021) (A. Pourfaraj et al., 2020). The inverter of a PV based system, which is a freestanding unit, converts standalone DC electricity to AC while charging the power storage unit. Simultaneously, the PV system's DC-DC converter is optimized to draw maximum energy from the PV panels and supply a sufficiently high DC voltage to the inverter (R. Kumar et al., 2023).The output waveform quality is significantly influenced by the modulation approach used to regulate the inverter output (L. Zhang et al., 2016). Sinusoidal Pulse Width Modulation (SPWM), one of the several modulation methods available for voltage source inverters, is widely recognised for being straightforward and simple to manage. This paper focuses on the analysis and design of various levels of Multilevel inverters with Cascaded H-bridge Multilevel Inverters using MATLAB Simulink and by using two different methods for pulse generation (with and without PWM). This study assesses total harmonic distortion for different levels of MLI. This paper is organised as follows: Section II explains the previous work done related to this report. Section III discusses, in brief, the modelling of a Multilevel Inverter in MATLAB. Section IV describes the THD Analysis of the MLI. Section V concludes the work.

II. LITERATURE REVIEW

Over the past few years, multilevel inverter (MLI) topologies—especially cascaded structures—have seen significant advancements aimed at improving harmonic performance and reducing the number of switching devices. Both symmetric and asymmetric inverter designs offer unique benefits, but when it comes to harmonic reduction, asymmetric configurations often have the upper hand. With these designs it is possible to achieve higher output voltage levels using fewer switches which results in a lower total harmonic distortion (THD). Asymmetric MLI (M. A. Al-Hitmi et al., 2023) reduces the number of components to increase system efficiency while providing better quality of harmonics than symmetric MLI.

Breakthroughs in inverter designs can be observed in the work of T. Roy et al. (2021) who constructed a 7-level switched-capacitor inverter. This topology eliminates magnetic components, thus reducing the switch count and the voltage stress across the components. The design is attributed to being compact and efficient which is especially useful for low to medium power modular cascaded systems that are space constrained. Reliability is another critical issue concerning inverter applications. To solve this problem, A. Akbari et al. (2022) proposed a new topology aimed at greater system reliability by reducing active components and incorporating fault tolerant designs. The inverter is able to operate under the faults without performance loss as the harmonic distortion remains within limitations, therefore making it ideal for robust cascaded MLI systems.

(R. Sun et. al, 2022) developed a multi-level inverter utilizing combining switched-capacitor and flying-capacitor fed T-type units which improved harmonic characteristics and voltage levels. The modulation technique used is easily scalable and provides high-quality waveforms. Additionally, a dual-mode interleaved multilevel inverter for photovoltaic (PV) systems was created by (A. Pourfaraj et al., 2020). This topology improves the overall conversion efficiency and THD. Its dual operation mode enables better voltage balancing and smoother waveform synthesis which is advantageous for cascaded inverters in solar energy systems.

III. RESEARCH METHOD

A. Three Level Cascaded Inverter

In a three level inverter, a pulse generator has been used for all four MOSFETs with 50 Hz as base frequency as shown in Fig. 1. A phase delay of 0.001 second is

provided to a single alternate pair of MOSFET. Based on the switching logic each gate is provided with the required pulse width percentage. The waveform output is shown in Fig. 2. The input voltage is 230 volts. For switching configuration of SPWM, the three level cascaded inverter, an output frequency of 50 Hz by using a sine generator and repeating signal has been provided. Output of these blocks is compared with a greater than block which is then given to one leg MOSFETs in the H-bridge cell and the other pair gets negative one gain of the signal as shown in Fig. 3. To attain the modulation index of one. Carrier frequency of 1 kHz and reference sine frequency of 50 Hz is fixed (B. Sakthisudhursun et al., 2016). For amplitude 0 to 1 of the sine wave, amplitude needs to be fixed for the carrier as [0 1 0] with 1 kHz as frequency. This shifts the harmonics of the sine wave to a higher frequency range of 1 kHz (Jae Hyeong Seo et al., 2001).

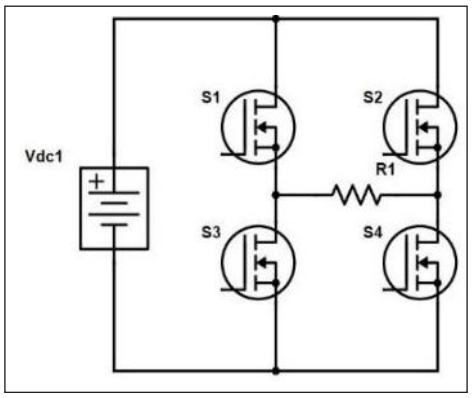

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Fig. 1: III Level Inverter

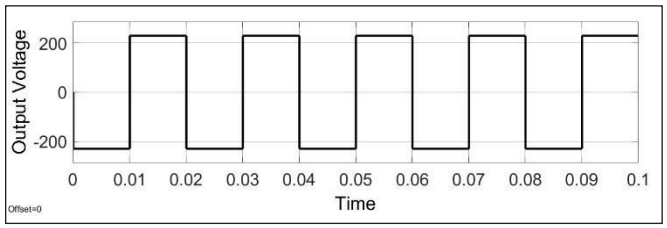

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Fig. 2: Output Voltage of III Level MLI Using Pulse Generator Method

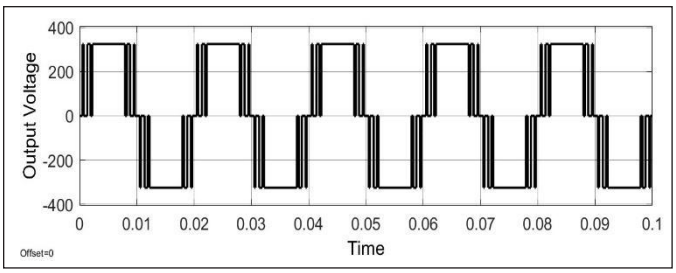

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Fig. 3: Output Voltage of III Level MLI Using SPWM Method

B. Five Level Cascaded Inverter

In a five level cascaded inverter, two individual cells are connected in a cascaded order, providing five levels voltage output (V. Anand et al., 2023). Each cascaded inverter together consists of eight MOSFETs. Using or gate is required to generate pulse width with two pulse generators (M. G. Marangalu et al., 2023). For generating S2 gate, (i) pulse width = 12.5% and delay = 0, (ii) pulse width = 50% and delay = 0.01s. These cascaded inverters operate for a frequency of 50 Hz (A. Dekka et al., 2020). Circuit is given as Fig. 8 and the output voltage waveform is given as Fig. 9. Total input DC voltage provided is 375.5884 v. For switching configuration of SPWM, five level cascaded inverter, an output time frequency of 50 Hz by using a sine generator and repeating signal has been provided. Output of this is compared with a greater than block which is then given to one leg MOSFETs in the H-bridge cell and the other pair gets negative one gain of the signal as shown in Fig. 4. To attain a modulation index of one. Carrier frequency of 1 kHz and reference sine frequency of 50 Hz is fixed. For amplitude 0 to 2 of the sine wave, amplitude needs to be fixed for the carrier as [0 1 0], [1 2 1] with 1 kHz as frequency. This shifts the harmonics of the sine wave to the higher frequency range of 1kHz.

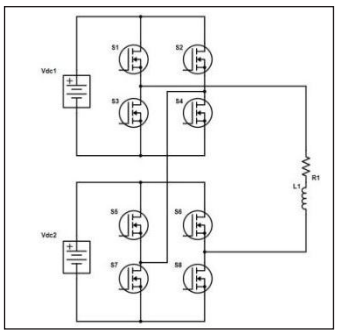

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Fig. 4: V Level Inverter

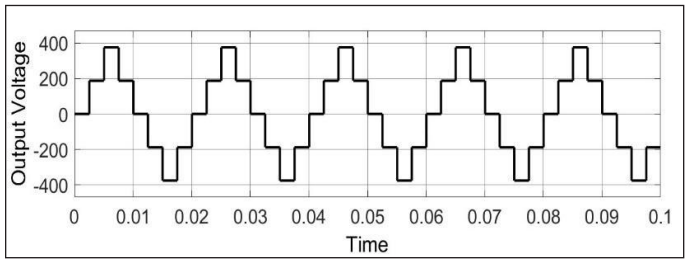

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Fig. 5: Output Voltage of V Level MLI Using Pulse Generator Method

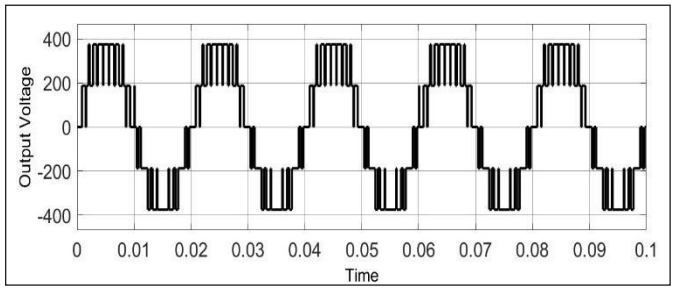

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Fig. 6: Output Voltage of V Level MLI using SPWM Method

C. Seven Level Cascaded Inverter

For seven level cascaded inverter, three individual cells are connected in a cascaded order, providing seven levels of voltage output. Each cascaded inverter together consists of twelve MOSFETs, four each (S. Alyami et al., 2021). Using an OR gate is required to generate pulse width with two pulse generators. For generating the S11 gate, (i) pulse width = 25% and delay = 0, (ii) pulse width = 66.66% and delay = 0.0066s. All three cells each operate for a frequency of 50 Hz together. The circuit is given in Fig. 7 and the output voltage waveform is given in Fig. 8. The total input voltage is 387.7456 v.

For switching configuration of SPWM, a seven level cascaded inverter, an output frequency of 50 Hz by using a sine generator and repeating signal has been given. Output of this is compared with a greater than block which is then given to one leg MOSFETs in each H-bridge cell and the other pair gets negative one gain of the signal as shown in Fig. 9. To attain a modulation index of one. Carrier frequency of 1 kHz and reference sine frequency of 50Hz is fixed. For amplitude 0 to 3 of the sine wave, amplitude needs to be fixed for the carrier as [0 1 0],[1 2 1],[2 3 2] with 1 kHz as frequency. This shifts the harmonics of the sine wave to a higher frequency range of 1 kHz.

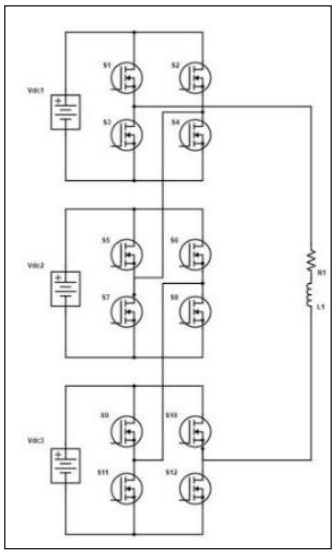

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Fig. 7: VII Level Inverter

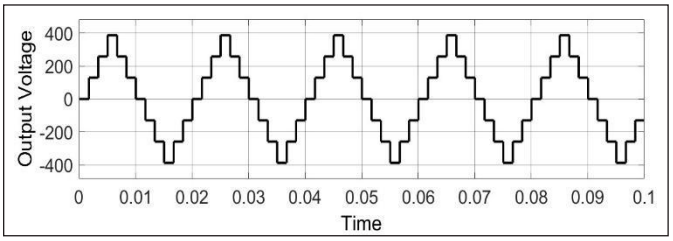

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Fig. 8: Output Voltage of VII Level MLI Using Pulse Generator Method

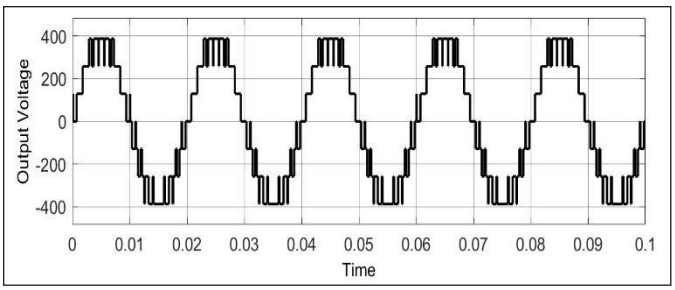

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Fig. 9: Output Voltage of VII Level MLI Using SPWM Method

D. Nine Level Cascaded Inverter

For nine level cascaded inverter, four individual cells are connected in a cascaded order, providing nine levels of voltage output. Each cascaded inverter together consists of sixteen MOSFETs, four each. Using an OR gate is required to generate pulse width with two pulse generators. For generating S15 gate, (i) pulse width = 25% and delay = 0, (ii). pulse width = 68.75% and delay = 0.00625 s. All four cells each operate for a frequency of 50 Hz together. The diagram is given in Fig. 10 and the waveform output is given in Fig. 11. The given input voltage is 392.2893 v.

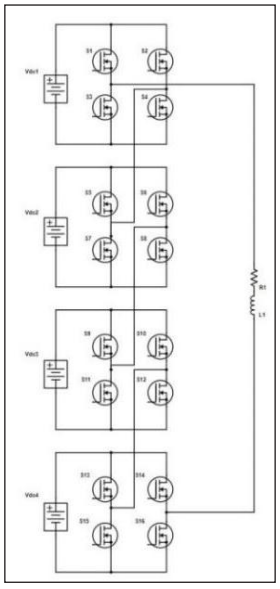

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Fig. 10: IX Level Inverter

For switching configuration of SPWM, nine level cascaded inverter, an output frequency of 50 Hz by using a sine generator and repeating signal has been provided. Output of this is compared with a greater than block which is then given to one leg MOSFETs in each H-bridge cell and the other pair gets negative one gain of the signal as shown in Fig. 12. To attain a modulation index of one. Carrier frequency of 1 kHz and reference sine frequency of 50 Hz is fixed. For amplitude 0 to 4 of sine wave amplitudes need to be fixed for the carrier as [0 1 0],[1 2 1],[2 3 2],[3 4 3] with 1 kHz as frequency. this shifts the harmonics of the sine wave to the higher frequency range of 1 kHz.

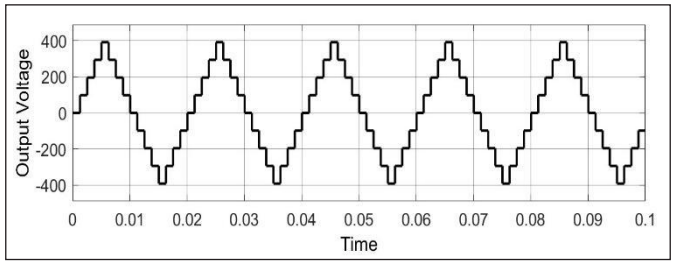

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Fig. 11: Output Voltage of IX Level MLI Using Pulse Generator Method

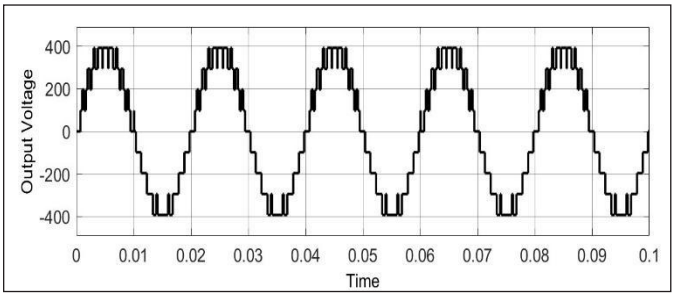

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Fig. 12: Output Voltage of IX Level MLI Using SPWM Method

E. Eleven Level Cascaded Inverter

In eleven level cascaded inverter, five individual cells are connected in a cascaded order, providing eleven levels of voltage output. Each cascaded inverter together consists of a total twenty MOSFETs, four each. Using an OR gate is required to generate pulse width with two pulse generators. For generating the S7 gate, (i) pulse width = 15% and delay = 0, (ii) Pulse width = 60% and delay = 0.008s. All five cells each will operate for a frequency of 50 Hz together. The diagram is given in Fig. 13 and the waveform output is given in Fig. 14. The given input voltage is 392.2893 v.

For switching configuration of SPWM, eleven level cascaded inverter, an output frequency of 50 Hz by using a sine generator and repeating signal has been provided. Output of this is compared with a greater than block which is then given to one leg MOSFETs in each H-bridge cell and the other pair gets negative one gain of the signal as shown in Fig. 15. To attain a modulation index of one. Carrier frequency of 1 kHz and reference sine frequency of 50 Hz is fixed. For amplitude 0 to 5 of sine wave amplitudes need to be fixed for the carrier as [0 1 0],[1 2 1],[2 3 2],[3 4 3],[4 5 4] with 1 kHz as frequency. This shifts the harmonics of the sine wave to a higher frequency range of 1 kHz.

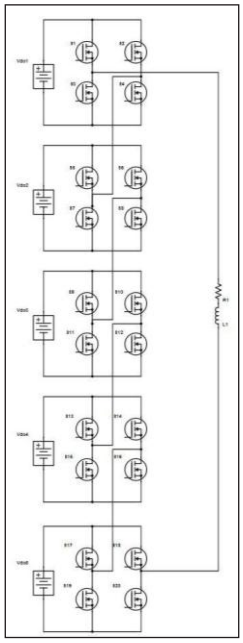

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Fig. 13: XI Level Inverter

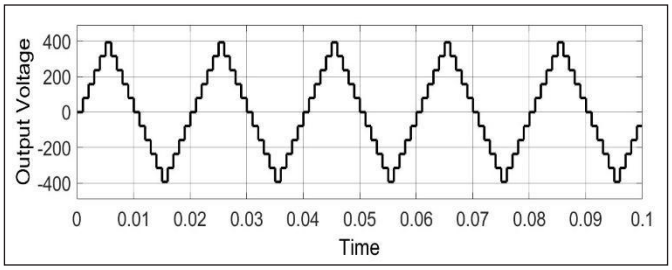

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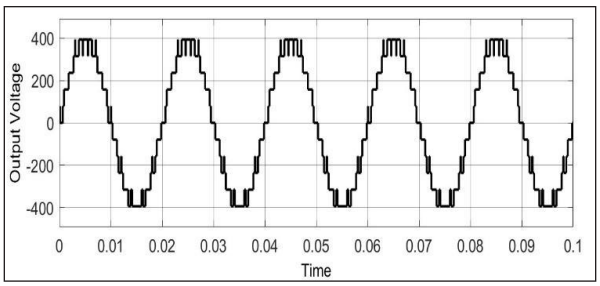
Fig. 14: Output Voltage of XI Level MLI Using Pulse Generator Method



Source: Authors own creation.

Fig. 15: Output Voltage of XI Level MLI Using SPWM Method

F. Thirteen Level Cascaded Inverter

In thirteen level cascaded inverter, six individual cells are connected in a cascaded order, providing thirteen levels of voltages output. Each cascaded inverter together consists of a total twenty-four MOSFETs, four each. Using an OR gate is required to generate pulse width with two pulse generators. For generating the S11 gate, (i) pulse width = 12.5% and delay = 0, (ii) pulse width = 58.33% and delay = 0.008333 s. All five cells together will operate for a time period of 20 ms. The diagram is given in Fig. 16 and the waveform output is given in Fig. 17. The given input voltage is 395.6337 v (V. Anand et al., 2022).

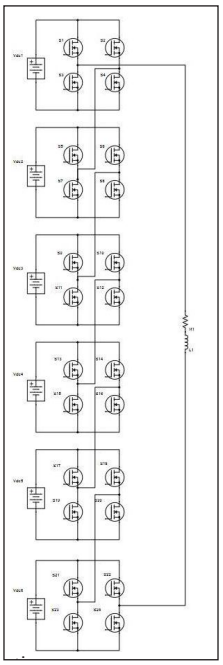


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Fig. 16: XII Level Inverter

For switching configuration of SPWM, the thirteen level cascaded inverter, an output frequency of 50 Hz by using a sine generator and repeating signal is provided. Output of this is compared with a greater than block which is then given to one leg MOSFETs in each H-bridge cell and the other pair gets negative one gain of the signal as shown in Fig. 18. To attain a modulation index of one. Carrier frequency of 1kHz and reference sine frequency of 50 Hz is fixed (K. Suresh et al., 2022). For amplitude 0 to 6 of the sine wave amplitudes need to be fixed for the carrier as [0 1 0], [1 2 1], [2 3 2], [3 4 3], [4 5 4], [5 6 5] with 1 kHz as frequency. This shifts the harmonics of the sine wave to a higher frequency range of 1 kHz.

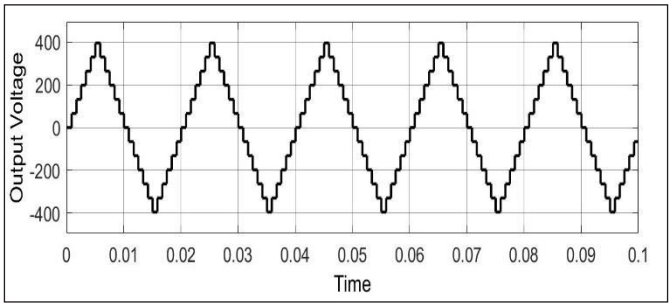

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Fig. 17: Output Voltage of XIII Level MLI Using Pulse Generator Method

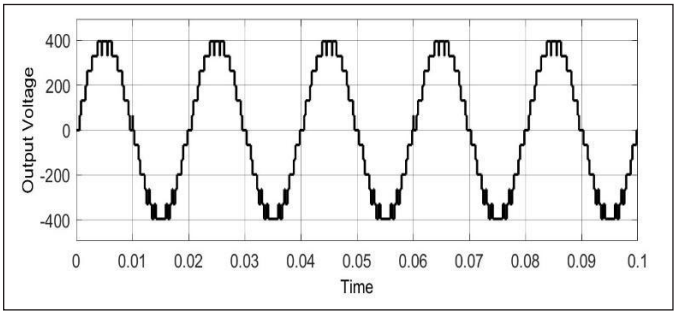

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Fig. 18: Output Voltage of XIII Level MLI Using SPWM Method

IV. RESULT AND ANALYSIS

A. Mathematical Expression

Output voltage is being analyzed using this Fourier series. It represents voltage waveform in terms of sine and cosine terms. This series is then used to find the fundamental harmonics and respective higher order harmonics. It is also used to find THD.

$$V(t) = a_0/2 + \Sigma(a_0 \cos(nwt) + b_n \sin(nwt)) \quad (1)$$

where: V(t) is the inverter output function being represented. $a_n/2$ is the average value of the function over a period. Σ denotes the summation over all integers n. a_n and b_n are the Fourier coefficients given by the following formulas:

$$a_n = (2/\pi) \int[0,2\pi] V(t) \cos(nwt) \quad (2)$$

$$b_n = (2/\pi) \int[0,2\pi] V(t) \sin(nwt)\, dx \quad (3)$$

equation (1) can also we represented as,

$$V(x) = \Sigma(c_n\, e^{\wedge}(i*nwt)) \quad (4)$$

Where c_n represents the complex Fourier coefficients, given by:

$$c_n = (1/2\pi) \int[0,2\pi] V(t)\, e^{\wedge}(-i*nwt)\, dx \quad (5)$$

$$THD = \text{sqrt}\ ((V_2^2 + V_3^2 + \ldots + V_n^2) / V_1^2) * 100 \quad (6)$$

where: V_2, V_3, ..., V_n are the RMS voltage values of the harmonic components (excluding the fundamental).V_1 is the RMS voltage value of the fundamental component.

Using equations (1), (2), (3) & (4). Following results have been verified for manual calculation in Table 1.

Table 1: MATLAB Code Output for Manual Verification

Manual for V fundamental	an	bn	VFUND(PEAK)	VFUND(RMS)
3 LEVEL	-220	4.04E-14	220	155.5635
5 LEVEL	-226.6876523	226.6876523	320.5848	226.6877
7 LEVEL	-160.7873644	278.4918844	321.5747	227.3877
9 LEVEL	-123.2607181	297.5776974	322.0958	227.7561
11 LEVEL	-99.61753798	306.5912567	322.3691	227.9494
13 LEVEL	-83.47600844	311.5367047	322.5265	228.0607

Source: Authors own creation.

Table 2: Harmonic Analysis for Multilevel Inverter with R Load Using Pulse Generator

R Load	VTHD	SOURCE	SWITCH	VDC	VOUT(RMS)	VOUT(PEAK)	VFUND	VFUND(RMS)
Simple Inv	48.31	1	4	230	229.9	229.9	292.7	207
5 LEVEL	28.99	2	8	375.5884	229.8	375.3	312.2	220.7
7 LEVEL	21.72	3	12	387.7456	230.2	387.3	318.2	225
9 LEVEL	18.16	4	16	392.2893	229.7	391.7	319.6	226
11 LEVEL	16.26	5	20	394.4467	229.6	393.7	320.5	226.6
13 LEVEL	15.18	6	24	395.6337	229.6	394.7	321.1	227.1

Source: Authors own creation.

Table 3: Harmonic Analysis for Multilevel Inverter with RL Load Using Pulse Generator

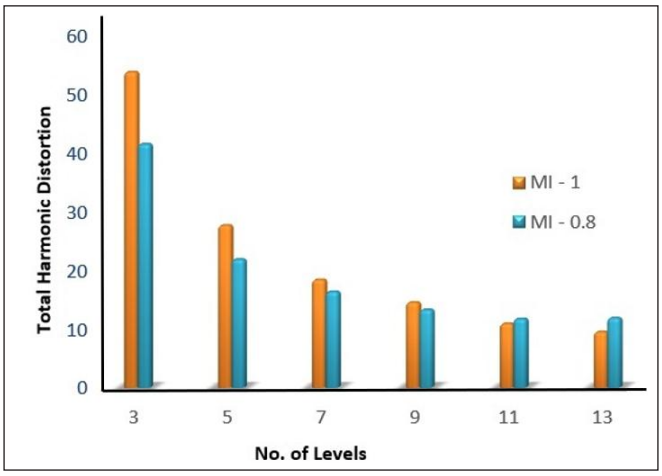
RL Load	VTHD	ITHD	SOURCE	SWITCH	VDC	VOUT(RMS)	VOUT(PEAK)	VFUND	VFUND(RMS)
Simple Inv	48.31	47.92	1	4	230	229.9	229.9	292.7	207
5 LEVEL	28.99	28.61	2	8	375.5884	229.8	375.3	312.2	220.7
7 LEVEL	21.72	21.37	3	12	387.7456	230.2	387.3	318.2	225
9 LEVEL	18.16	17.84	4	16	392.2893	229.7	391.7	319.6	226
11 LEVEL	16.26	15.98	5	20	394.4467	229.6	393.7	320.5	226.6
13 LEVEL	15.18	14.93	6	24	395.6337	229.6	394.7	321.1	227.1

Source: Authors own creation.

Table 4: Harmonic Analysis for Multilevel Inverter with R Load Using SPWM

SPWM R Load	THD(MI=1)	THD(MI=0.8)
3 LEVEL	52.55	40.56
5 LEVEL	27.01	21.37
7 LEVEL	17.97	15.99
9 LEVEL	14.21	12.99
11 LEVEL	10.67	11.46
13 LEVEL	9.3	11.61

Source: Authors own creation.



Source: Authors own creation.

Fig. 19: A Bar Chart Comparing Total Harmonic Distortion for Modulation Index of 1 and 0.8

An understanding of the harmonic content in the output waveform of a multilevel inverter with R load and RL load may be gained by doing a harmonic analysis. The output voltage, current quality and ascertained the effect on the system's performance by examining the harmonic components has been evaluated. Thus in Table 2, the voltage harmonic decreases as the level of the inverter increases and a constant output RMS voltage of 230V has been maintained. In Table 3 with RL load, the voltage harmonic is not affected but the current harmonic will change due to the inherent property of the inductor. Here also the harmonic decreases with increase in the level of the inverter. Table 4 shows the result of the same MLI but the pulse is generated using SPWM and modulation index 1 and 0.8 are used. As a result, it has been confirmed that the THD (total harmonic distortion) of voltage and current, fundamental voltage (peak and RMS), output and input voltages (peak and RMS), and the number of sources and switches for all levels for R and RL load conditions are comparable.

V. CONCLUSION

The analysis of THD and harmonics of a cascaded H bridge multilevel inverter arrangement reveals that increasing the inverter's level leads to a significant decrease in voltage and current harmonics, indicating superior harmonic suppression capabilities. Even when considering RL loads, the voltage harmonics remain unaffected while the current harmonics change due to the properties of the inductor. The comparison of THD for voltage and current confirms that higher-level inverters exhibit lower distortion levels. These findings emphasize the effectiveness of multilevel inverters in mitigating harmonic distortions and improving the overall performance and output quality of power electronic systems, renewable energy systems, and motor drives.

VI. IMPLICATION

This document describes essential information on motors drives, industrial applications, and renewable energy systems related to CHB-MLIs. One of the applications of this research is that increasing the number of voltage levels results in significant power quality improvements by reducing total harmonic distortion (THD) of current and voltage. This means that higher level CHB-MLIs are suitable for grid tied solar and wind systems since these systems require high quality output waveforms.

The research also confirms the effectiveness of SPWM oscillations with low modulation indexes since it provides complete control over harmonic distortion and accurate command of control. Current harmonics vary with the inductive nature of RL load systems while voltage harmonics remain constant. This should bring forward the

need to look at different types of loads while designing systems.

In addition, for systems which are easier to deploy on large scales and distributed around the world, the lightweight structure of CHB inverters provides important benefits since they require lesser components compared to other topologies.

VII. LIMITATION AND FUTURE RESEARCH

The study presents some results, but not without a number of obvious limitations. Perhaps most significantly, all simulations in this study were conducted using MATLAB Simulink, which is an advanced model and a powerful analysis tool. However, it does not capture real-world hardware nuances such as switching losses, temperature variations, electromagnetic interference, parasitic effects, and many others which certainly impact the performance of the inverter.

Also, another limitation seems to be the consideration of only ideal R and RL loads. In most real-life scenarios, electrical loads are far more complex and may be non-linear, unbalanced, or change with time. The behavior of the inverter under these conditions is not studied in this case which limits the scope of the study's conclusions.

Furthermore, the study concentrates solely on Sinusoidal Pulse Width Modulation (SPWM) as the pulse generation technique. While SPWM is straightforward and widely used, other techniques such as Space Vector Modulation (SVM) or Selective Harmonic Elimination (SHE) are more sophisticated and could provide better solutions but were ignored.

Important practical concerns are also omitted, such as handling of faults, heat dissipation, and aging of the components. For these concerns, the responsive long-term functionality of inverters in real systems depends on these issues.

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