FPGA Design of Optimized CIC Interpolator for DSP based Wireless Communication Systems

Rajesh Mehra*

Abstract

In this paper an efficient multiplier less technique is presented to design and implement a high speed CIC interpolator for wireless applications like SDR and GSM. The implementation is based on efficient utilization of embedded LUTs of the target device to enhance the speed of proposed design. It is an efficient method used to design and implement CIC interpolator because the use of embedded LUTs not only increases the speed but also saves the resources on the target device. The fully pipelined CIC interpolator has been designed with Matlab, simulated with Modelsim, synthesized with Xilinx Synthesis Tool (XST), and implemented on Spartan-3E based XC3s500e-4fg320 target device. The proposed design can be operated at an estimated frequency of 166.5 MHz by consuming very less resources available on target device to provide cost effective solution for wireless communication systems. The power consumption of the proposed design has been 0.08098W at 27.1 degree C junction temperature.

Keywords : CIC, FPGA, GSM, LUT, SDR

1. Introduction

The widespread use of digital representation of signals for transmission and storage has created challenges in the area of digital signal processing [1]. The applications of digital FIR filter and up/down sampling techniques are found everywhere in modem electronic products. For every electronic product, lower circuit complexity is always an important design target since it reduces the cost [2]. There are many applications where the sampling rate must be changed. Interpolators and decimators are utilized to increase or decrease the sampling rate. Up sampler and down sampler are used to change the sampling rate of digital signal in multi rate DSP systems. This rate conversion requirement leads to production of undesired signals associated with aliasing and imaging errors. So some kind of filter should be placed to attenuate these errors [3]. Recently, there is increasingly strong interest on implementing multi-mode terminals, which are able to process different types of signals, e.g. WCDMA, GPRS, WLAN and Bluetooth. These versatile mobile terminals favor simple receiver architectures because otherwise they'd be too costly and bulky for practical applications [4]. The answer to the diverse range of requirements is the software defined radio. Software defined radios (SDR) are highly configurable hardware platforms that provide the technology for realizing the rapidly expanding digital wireless

---

*National Institute of Technical Teachers' Training & Research, Chandigarh, INDIA.

communication infrastructure. Many sophisticated signal processing tasks are performed in SDR, including advanced compression algorithms, power control, channel estimation, equalization, forward error control, adaptive antennas, rake processing in a WCDMA (wideband code division multiple access) system and protocol management. Today's consumer electronics such as cellular phones and other multi-media and wireless devices often require digital signal processing (DSP) algorithms for several crucial operations[5] in order to increase speed, reduce area and power consumption. Due to a growing demand for such complex DSP applications, high performance, low-cost Soc implementations of DSP algorithms are receiving increased attention among researchers and design engineers. Although ASICs and DSP chips have been the traditional solution for high performance applications, now the technology and the market demands are looking for changes.

On one hand, high development costs and time-to-market factors associated with ASICs can be prohibitive for certain applications while, on the other hand, programmable DSP processors can be unable to meet desired performance due to their sequential-execution architecture [6]. In this context, embedded FPGAs offer a very attractive solution that balance high flexibility, time-to-market, cost and performance. The digital signal processing application by using variable sampling rates can improve the flexibility of a software defined radio. It reduces the need for expensive anti-aliasing analog filters and enables processing of different types of signals with different sampling rates [7]. It allows partitioning of the high-speed processing into parallel multiple lower speed processing tasks which can lead to a significant saving in computational power and cost. Wideband receivers take advantage of multirate signal processing for efficient channelization and offers flexibility for symbol synchronization.

2. CIC Interpolator

The two basic building blocks of a CIC filter are an integrator and a comb [8]-[11]. An integrator is simply a single-pole IIR filter with a unity feedback coefficient:

$$y[n] = y[n-1] + x[n] \tag{1}$$

This system is also known as an accumulator. The transfer function for an integrator on the z-plane is:

$$H_I(z) = \frac{1}{1 - z^{-1}} \tag{2}$$

The power response of integrator is basically a low-pass filter with a -20 dB per decade (-6 dB per octave) rolloff, but with infinite gain at DC. This is due to the single pole at z = 1; the output can grow without bound for a bounded input. In other words, a single integrator by itself is unstable and shown in Fig. 1.

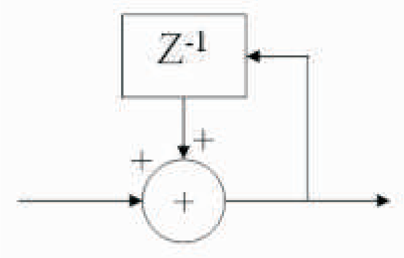


Fig 1 : Basic Integrator

A comb filter running at the high sampling rate, fs, for a rate change of R is an odd symmetric FIR filter described by:

$$y[n] = x[n] - x[n - RM] \tag{3}$$

Where M is a design parameter and is called the differential delay. M can be any positive integer, but it is usually limited to 1 or 2. The corresponding transfer at fs

$$H_c(z) = 1 - z^{-RM} \tag{4}$$

When R = 1 and M = 1, the power response is a high-pass function with 20 dB per decade (6 dB per octave) gain (after all, it is the inverse of an integrator). When RM $\neq$ 1, the power response takes on the familiar raised cosine form with RM cycles from 0 to 2π. The basic comb is shown in Fig.2.When we build a CIC filter, we cascade, or chain output to input, N integrator sections together with N comb sections. This filter would be fine, but we can simplify it by combining it with the rate changer.

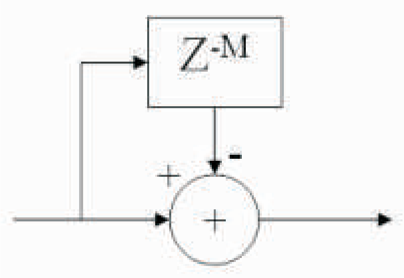


Fig 2 : Basic Comb

Using a technique for multirate analysis of LTI systems from, we can "push" the comb sections through the rate changer, and have them become at the slower sampling rate fs/R.

$$y[n] = x[n] - x[n - M] \tag{5}$$

A CIC interpolator would have N cascaded comb stages running at fs/R, followed by a zero-stuffer, followed by N cascaded integrator stages running at fs. The transfer function for a CIC filter at fs is

$$H(z) = H_I^N(z) H_C^N(z)$$
$$H(z) = \frac{(1 - z^{-RM})^N}{(1 - z^{-1})^N} = (\sum_{k=0}^{RM-1} z^{-k})^N \tag{6}$$

This equation shows that even though a CIC has integrators in it, which by themselves have an infinite impulse response, a CIC filter is equivalent to N FIR filters, each having a rectangular impulse response. Since all of the coefficients of these FIR filters are unity, and therefore symmetric, a CIC filter also has a linear phase response and constant group delay. The magnitude response at the output of the filter may be expressed as:

$$|H(f)| \quad \left| \frac{Sin \quad MF}{Sin \frac{f}{R}} \right|^N \tag{7}$$

By using the relation sin x ≈ x for small x and some algebra, we can approximate this function for large R as:

$$|H(f)| \approx \left| RM \frac{Sin \pi MF}{\pi MF} \right|^N for 0 \le f \le \frac{1}{M} \tag{8}$$

We can notice a few things about the response. One is that the output spectrum has nulls at multiples of f = 1/M. In addition, the region around the null is where aliasing/imaging occurs. If we define fc to be the cutoff of the usable pass band, then the aliasing/imaging regions are at:

$$(i - f_c) \le f \le (i + f_c) \tag{9}$$

For $f \le \frac{1}{2}$ and i = 1, 2,……[R/2]. If $f_c \le \frac{M}{2}$

The maximum of these will occur at the lower edge of the first band i.e. 1-fc which can be used to adjust R, M, and N as required. The pass band attenuation is a function of the number of stages. So increase in the number of stages improves the imaging/alias rejection, it also increases the pass band droop.

3. CIC Interpolator Design & Simulation

In this proposed work, first of all a CIC interpolator is designed using Matlab [12] by taking R = 8, N=3 and M=2 whose output is shown in Fig3.

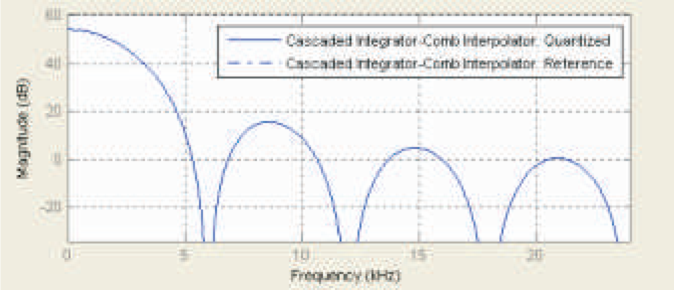


Fig 3 : Cascaded Integrator Comb Interpolator

The proposed design is implemented using 3 stages to accomplish three things. First, we have slowed down half of the filter and therefore increased efficiency. Second, we have reduced the number of delay elements needed in the comb sections. Third, and most important, the integrator and comb structure are now independent of the rate change. This means we can design a CIC filter with a programmable rate change and keep the same filtering structure.

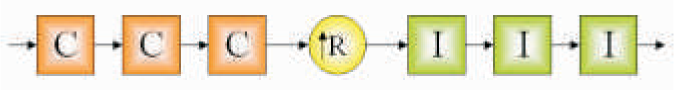


Fig 4 : CIC Interpolator with 3 stages

The structure of CIC interpolator shown in Fig.4 has been realized by developing the equivalent VHDL code for the filter then its verification and behavioral simulation was done with the help of Modelsim simulator. The zoom in and zoom out view of Modelsim based interpolator responses are shown in Fig.5 and Fig.6 respectively.

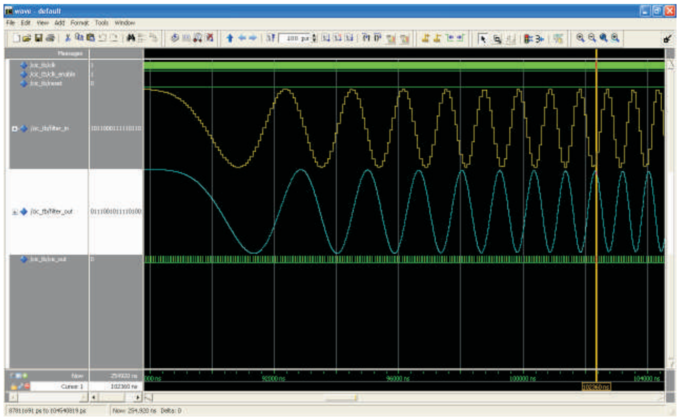


Fig 5 : Zoom In View of Proposed Interpolator

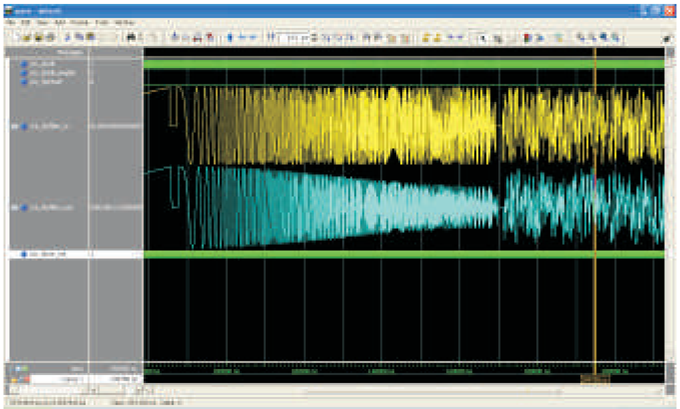
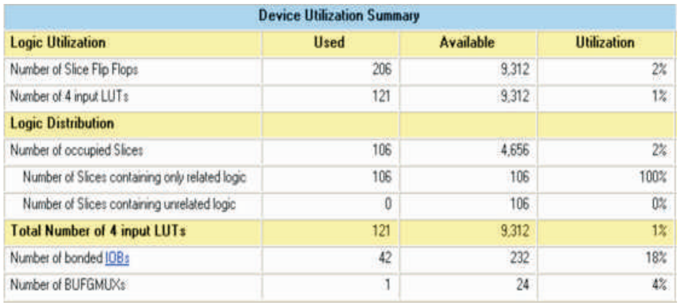


Fig 6 : Zoom Out View of Proposed Interpolator

4. FPGA Implementation Results

To observe the speed and resource utilization, RTL has been generated, verified and synthesized using Xilinx Synthesis Tool (XST). The proposed CIC interpolator filter has been implemented on Spartan-3E based XC3s500e-4fg320 target device using fully pipelined LUT based multiplier less technique. The resource utilization of proposed implementation is shown in table1.

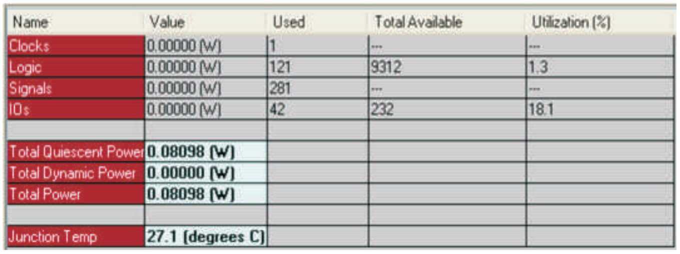
Table 1 : Spartan-3E Based Resource Utilization



Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	206	9,312	2%
Number of 4 input LUTs	121	9,312	1%
Logic Distribution			
Number of occupied Slices	106	4,656	2%
Number of Slices containing only related logic	106	106	100%
Number of Slices containing unrelated logic	0	106	0%
Total Number of 4 input LUTs	121	9,312	1%
Number of bonded IOBs	42	232	18%
Number of BUFGMUXs	1	24	4%

The proposed design shows an efficient realization of CIC interpolator by using embedded LUTs of target FPGA to provide high speed operation. The LUT based proposed design can operate at a maximum frequency of 166.5 MHz by consuming very less resources of target FPGA device. The proposed design consumes total power of 0.08098W at 27.1 degree C junction temperature as shown in table 2.

Table 2 : Power Consumption



Name	Value	Used	Total Available	Utilization (%)
Clocks	0.00000 (W)	1	---	---
Logic	0.00000 (W)	121	9312	1.3
Signals	0.00000 (W)	281	---	---
IOs	0.00000 (W)	42	232	18.1
Total Quiescent Power	**0.08098 (W)**			
Total Dynamic Power	**0.00000 (W)**			
Total Power	**0.08098 (W)**			
Junction Temp	**27.1 (degrees C)**			

5. Conclusions

In this paper, a fully pipelined multiplier less approach has been presented to design and implement a CIC interpolator using embedded LUTs of target device. The results have shown enhanced performance in terms of speed and area utilization. The proposed transposed design can operate at a maximum frequency of 166.5 MHz by consuming considerably less resources available on target device to provide cost effective solution for SDR based wireless applications. The proposed design consumes total power of 0.08098W at 27.1 degree C junction temperature.

6. References

1. *Vijay Sundararajan, Keshab K. Parhi, "Synthesis of Minimum-Area Folded Architectures for Rectangular Multidimensional", IEEE TRANSACTIONS ON SIGNAL PROCESSING, pp. 1954-1965, VOL. 51, NO. 7, JULY 2003.*
2. *ShyhJye Jou, Kai-Yuan Jheng*, Hsiao-Yun Chen and An-Yeu Wu, "Multiplierless Multirate Decimator I Interpolator Module Generator", IEEE Asia-Pacific Conference on Advanced System Integrated Circuits, pp. 58-61, Aug-2004.*
3. *S K Mitra, Digital Signal Processing, Tata Mc Graw Hill, Third Edition, 2006.*
4. *Xinmiao Zhang, Jiangli Zhu, "High-throughput Interpolation Architecture for Algebraic Soft-decision Reed-Solomon Decoding" pp. 1-11. IEEE-2009.*
5. *Ali AI-Haj, "An Efficient Configurable Hardware Implementation of Fundamental Multirate Filter Banks", 5th International Multi-Conference on Systems, Signals and Devices, pp.1-5, IEEE SSD 2008.*
6. *Binming Luo, Yuanfu Zhao, and Zongmin Wang, "An Area-efficient Interpolator Applied in Audio DAC'Σ-ΔThird International IEEE Conference on Signal-Image Technologies and Internet-Based System, pp.538-541, 2008.*
7. *N.M.Zawawi, M.F.Ain, S.I.S.Hassan, M.A.Zakariya, C.Y.Hui and R.Hussin, "Implementing WCDMA Digital Up Converter In FPGA" IEEE INTERNATIONAL RF AND MICROWAVE CONFERENCE, pp. 91-95, RFM-2008.*
8. *F.J.A. de Aquino, C.A.F. da Rocha, and L.S. Resende, "Design of CIC filters for software radio system," IEEE International Conference on Acoustics, Speech, Signal Processing, May 2006.*
9. *R. Uusikartano, and J. Takala, "Power-efficient CIC decimator architecture for fs/4-downconverting digital receivers," IEEE International Midwest Symposium on Circuits and Systems, Dec. 2004.*
10. *W.A. Abu-Al-Saud, and G.L. Stuber, "Modified CIC filter for sample rate conversion in software radio systems," IEEE Signal Processing Letters, Vol. 10, Issue: 5, pp. 152-154, May 2003.*
11. *G.J. Dolecek, and J.D. Carmona, "A new cascaded modified CIC-cosine decimation filter," IEEE International Symposium on Circuits and Systems, May 2005.*
12. *Mathworks, " Users Guide Filter Design Toolbox 4", March-2007.*