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Ultra-thin Gate Oxide Tunneling in MOS Transistors: A Simulation Study by Minimos

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Abstract

Constant downscaling of gate oxide thickness in present state of art technology in MOS has motivated interest in the eventual tunneling that seriously limits and warns the faithful performance of MOS. In the present paper, with help of existing tunneling models of two very important gate leakage currents like Fowler-Nordheim and Direct tunnel such leakage are successfully simulated by Minimos-NT simulator under different conditions of gate and drain biases and verified the results with the experimental results.

Keywords: Saponification, Comparative, Physio Chemical Parameters, Trace metals, Heavy Metals, Oil Samples.

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1. Introduction

According to the National Technological Roadmap for Semiconductors (NTRS) [1], the scaling trend for gate dielectrics is such that for sub-100 nm generation devices, an equivalent gate oxide thickness of less than 2.0 nm will be required. With scaling of the gate oxide thickness current leakage through the gate terminal sets in. This is the result of an increased electric field across the gate oxide. Less is the thickness greater is the leakage. This is the tunneling phenomena (also known as the phenomenon of field emission) in which carriers' transition through classically forbidden energy states are described by quantum mechanics only. The reason lies in the wave nature of particles exhibited in the quantum scale. Tunneling may be seen from the substrate to gate or gate to substrate as well. A positive gate bias causes the channel electrons to tunnel through the oxide into the gate material while a negative gate bias causes the reverse; that is electrons from the polysilcon gate tunnel through the oxide into the channel. This increased current not only adversely affects the MOS device performance but also greatly increases the standby power consumption of a highly integrated chip. Tunneling adversely affects the device performance mainly through two significant factors. The increased off-state current increases the increased off-state power dissipation and the ROMs utilize the leakage current to erase charge on the floating contact e.g. FLASH and EEPROM. Tunneling between substrate and gate poly silicon occurs most importantly through the Fowler-Nordheim (FN) or through the direct mechanism. In FN mechanism the electrons close enough to the Fermi level of the semiconductor get through the oxide band gap and arrive at its conduction band. Theoretical analysis of strict accuracy for low voltage tunnel current still remains an open challenge in spite of a number of proposed

models of tunnel mechanisms are known for several decades [2-4].The drain induced barrier lowering (DIBL) effect has not been given due attention in the studies of direct tunneling [3-6] yet some authors have included the DIBL in the more logical analysis of the direct tunneling in ultra thin oxide layers of relatively short channel length [7-8]. In the present study, an n-MOS transistor with heavily doped n+ polysilicon gate is considered. In the present paperthe Fowler-Nordheim and Direct tunneling under different conditions of gate and drain voltages has been studied with use of existing models and their implementations in Minimos-NT. The channel length is restricted to a relatively large one because otherwise the gate silicon dioxide should be made still thinner to control the short channel effects and to get a good sub threshold turn-off slope. Gate tunneling assisted by drain induced lowering of barrier at the source end is also studied in our simulation.

1. Model

1.1 Tsu- Esaki model

The tunnel current through a barrier with the plateaus on either side at different energies is derived in the Tsu-Esaki model. An analytical expression of the gate tunneling current density is derived by approximating the original Tsu-Esaki integral.

$$J = \frac{4\pi m^* q}{h^3} \int_{E_{\min}}^{E_{\max}} T(E_y) N(E_y) dE_y \qquad (1)$$

$$N = \int_0^{\infty} [f_1(E) - f_2(E)] dE_\rho$$

f1 and *f2* be occupancy function near the interfaces and E_ρ transverse part of the total energy.

$T(E_y)$ = transmission coefficient.

N = Supply Function

$E_y = y$ part of the total energy.

$E_{\min}$ and $E_{\max}$ are the highest conduction band edges at the two opposite sides of the dielectric.

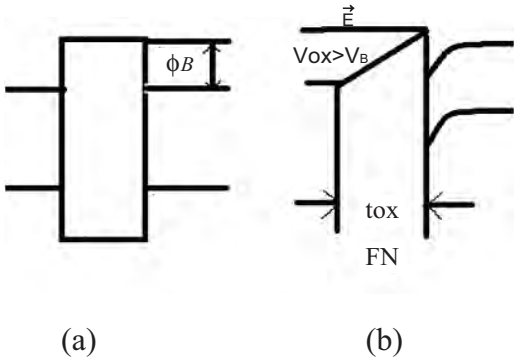
The Fowler-Nordheim or the direct tunneling current densities are calculated, using the Tsu-Esaki model, as the difference between the currents flowing from left to right and right to left of the potential barrier in the oxide layer. It is thus only the relative values of the oxide voltage and the barrier voltages that determine whether it is FN or direct tunneling.

1.2 Fowler- Nordheim (FN) Tunneling

In FN tunneling the electrons face a triangular potential barrier at the oxide-semiconductor interface. Ignoring the effects of finite temperature and the image-force induced barrier lowering the electron current density through the oxide layer is given by [9].

$$J_{FN} = \frac{q^3 \varepsilon_{ox}^2}{16\pi^2 \hbar \phi_B} \exp\left(\frac{-4\sqrt{2m^*}\phi_B^{3/2}}{3\hbar^2 q \varepsilon_{ox}}\right) \qquad (2)$$

ε_{ox} oxide field, ϕ_B = barrier height for the electrons in the conduction band and m = effective mass of conduction band electrons. The triangular potential barrier in FN tunneling equation is reflected through the validity of the equation for $V_{ox} > \phi_B$, V_{ox} being the voltage drop in the oxide layer. This corresponds to the observation that for such tunneling to x>= 4 nm. The energy band condition for equilibrium i.e. of no tunneling is shown in Fig. 1(a) while that for the FN tunneling is depicted in Fig.1(b).



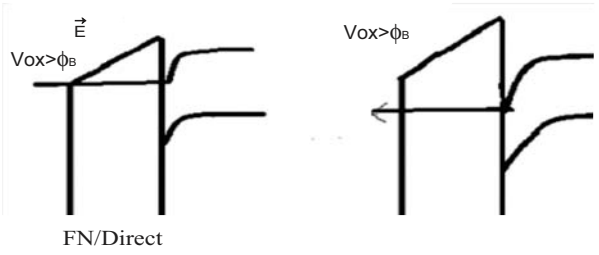
(a) (b)

Figure 1: Energy band schematic of a) equilibrium condition, $0_g V$=and b) Fowler-Nordheim, $Vg \neq 0, Vox > \phi_B$

In the simulation, the trap assisted tunnel TAT) through gate oxide of ~1.5 – 3.6 nm has been duly taken care of. There are many models for TAT. In case of repeated high electric field stress, developed during the high frequency erasing and rewriting in non-volatile memory cells, defects arise in the dielectric leading to the tunnel currents of hopping electrons between defects. Defects are modeled as single traps. The TAT may be considered as a two-step process. Firstly, electrons from the negative substrate are trapped and then they are de-trapped to the positive gate.

1.3 Direct Tunneling

Here for very thin oxide thickness (less than ~ 4 nm) the electrons in the inverted silicon tunnel straight into the gate material through the oxide band gap bypassing the conduction band of oxide layer. Unlike the FN, the electrons in direct tunneling face a trapezoidal potential barrier at the oxide-semiconductor interface. The trapezoidal potential barrier in direct tunneling equation is reflected through its validity condition that $V_{ox} < \Phi_B$. This corresponds to the observation that for such tunneling $t_{ox} < 4$ nm. The energy band condition of FN/direct is depicted in Fig.2(a) while that for direct tunneling is shown in Fig.2(b). In the present study we have considered the electron tunneling from the conduction band only where the gate to channel tunneling current in inversion and gate to body tunneling in accumulation is controlled. Schuegraf et al. derived a simplified analytical formula to represent direct tunnelling current assuming a trapezoidal barrier [10-11]. This simple theory did not, however, work well in the sub-1-V gate bias range. For better accuracy complicated band energies and quantum transport formalisms should be taken into consideration to simulate the design of the models.



(a) (b)

Figure 2: Energy band schematic of a) Fowler-Nordheim/Direct, $V_g = 0$, $V_{ox} = \phi_B$ and b) Direct tunneling. $V_g \neq 0$, $V_{ox} > \phi_B$

The electron current density through the oxide layer for direct tunneling is given by [11],

$$J_D = A\varepsilon_{ox}^2 \left(\frac{\phi_B}{V_{ox}}\right)\left(\frac{2\phi_B}{V_{ox}} - 1\right) e^{\frac{-B\left[1-\left(1-\frac{V_{ox}}{\eta_B}\right)^{\varsigma}\right]}{\varepsilon_{ox}}} \qquad (3)$$

$$A = \frac{q^{\varsigma}}{8\rho h \phi_B}$$

Φ_B being the barrier height.

3. Simulation and Results

The implementation of the tunneling models used in the present work is made in the device

simulator Minimos-NT, a user-oriented software tool developed at the Technical University, Vienna, Austria. The basic geometry of the device to show the various segments used in our simulation with the Minimos-NT are shown in Figure 3.

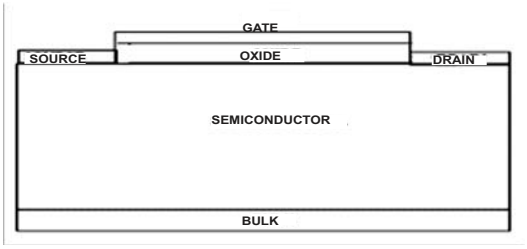
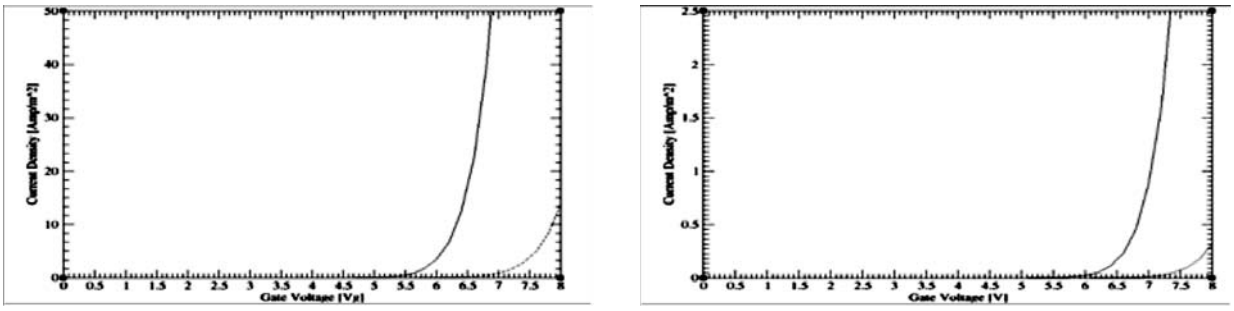


Figure 3: Basic geometry of the simulated MOS structure

Minimos-NT builds the consistent solution of the fundamental semiconductor equations in a hierarchial manner starting with a relatively simple model that is consistently refined by taking into account more complicated physical mechanisms. Here the set of equations for the electrostatic potential Ψ and the quasi-Fermi potential Φ_n of the electrons are solved iteratively following linearization of the equations. The derivatives in the partial differential equations are replaced by finite difference formulas at each node in a finite difference mesh. Dirichlet and Neumann boundary conditions are set by the Minimos-NT at the contacts and other segmental surfaces respectively. Proper grid allocation in the simulation domain is an important issue and is employed in the present software to maintain reasonable simulation time. We have taken an n-MOS as an example to study the various tunneling effects. At different oxide thicknesses and gate biases tunneling are examined in the MOS keeping its channel length and acceptor level at fixed values of 0.25 μmand $1x10^{16}$/c.c. respectively. For simulation of the tunnel current following the design models [9-11] the basic Tsu-Esaki tunnel mechanism is used wherein the trap assisted tunneling is considered. The effective oxide mass of electrons is taken as 0.5 and the trap concentration in the oxide layer is taken as 1e19 "cm^{-3}".



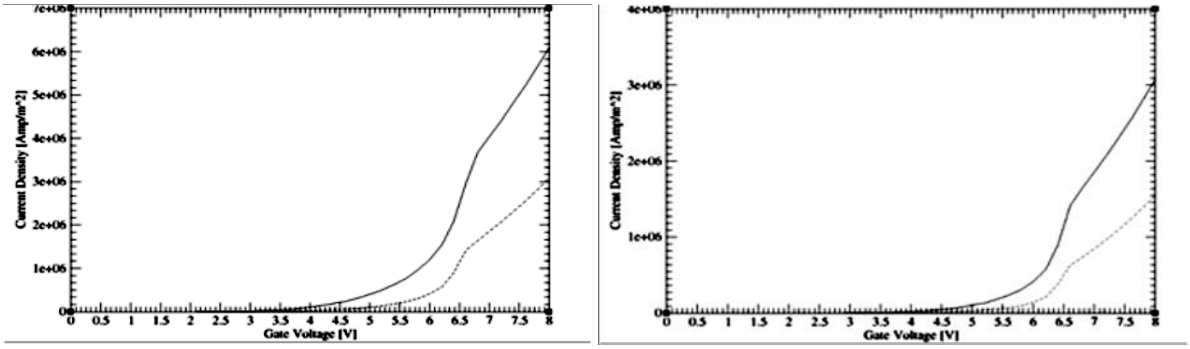
(a) **(b)**

Figure 4: Simulated FN tunnel current in thin oxide of thickness (a) t_{ox}= 4 nm (solid line) and 5 nm (dotted line) (b) t_{ox}= 5 nm (solid line) and 6 nm (dotted line), Drain Voltage = 0V.

In Figure 4 (a & b) we have plotted the current density vs the gate voltage using the FN tunneling model (equation 2). The parameters used are: oxide thicknesses: 4nm, 5nm and 6nm; drain voltage =0V. The tunnel leakage is seen to be very infinitesimal and insignificant. It is also observed that with increased thicknesses the leakage current appreciably falls and initiates at higher gate voltages. This is justified because of the wider barrier. The simulated results are seen to agree fairly well with the established experimental values. The surface

scattering is the limiting factor to degrade the mobility and results in such a poor tunnel current.

In the direct tunneling, we have considered only the electron tunneling from the conduction band itself and not from the valence band as the latter controls only the gate to body leakage in the depletion-inversion mode. Fig. 5 gives a plot of the direct tunneling current, on the basis of model equation 3 with varying gate voltages under the condition of zero drain bias. It is observed that the tunneling increases with gate voltage at a fixed value of oxide thickness and also increases with lowering thickness at a fixed value of gate voltage.

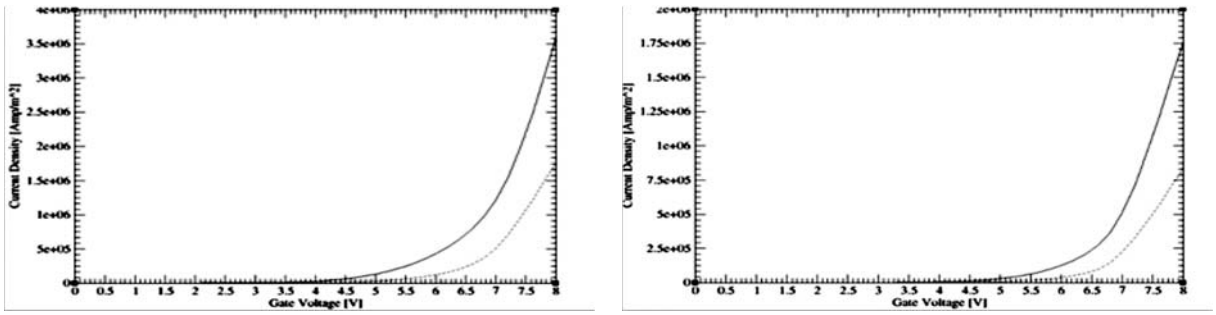


(a) **(b)**

Figure 5: Simulated direct tunnel current in ultra-thin oxide of thickness (a) t_{ox}=1 nm (solid line) and 1.25 nm (dotted line) (b) t_{ox}=1.25 nm, and 1.5 nm. Drain Voltage = 0V.

In Figure 6 we have shown the simulated results of the direct tunneling current in ultra-thin oxide for varying gate voltages under a non-zero drain voltage. The results show that the gate tunnel appreciable increases in case of finite and non-zero drain bias. This is quite justified because of the fact that the barrier at the source channel junction area is lowered by the positive drain. More is the drain bias more is the barrier lowering resulting in more tunnel leak.

The simulated results are all compared with the experimental results [12] and are seen to agree fairly well validates our phenomenological modeling and subsequent simulation with Minimos-NT.



(a) **(b)**

Figure 6: Simulated direct tunnel current in ultra-thin oxide of thickness (a) t_{ox}=1 nm (solid line) and 1.25 nm (dotted line) (b) t_{ox}=1.25 nm (solid line) and 1.5 nm (dotted line) Drain Voltage = 2V

4. Conclusions

On the basis of the results derived from the simulations on gate tunneling it is concluded that the FN tunneling is significantly very poor while the direct tunneling is appreciable especially in the case of extra thin gate oxide. The non-zerodrain voltage encourages and initiates the tunneling at lower gate voltage. The work may further have a scope to study the effect of image charge on the tunneling process. This would be done in our future simulations.

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