Implementation of Modified Carry Select Adder in Booth Multiplier

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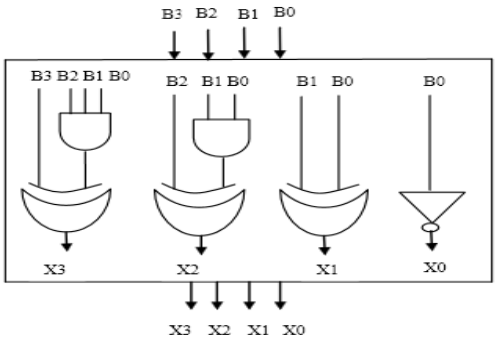
Abstract - *Design of area and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design, The Carry Select Adder (CSLA) provides a good compromise between cost and performance in carry propagation adder design. However, conventional CSLA is still area- consuming due to the dual ripple carry adder (RCA) structure. In this paper, modification is done at gate-level to reduce area and power consumption. The Modified Carry Select-Adder (MCSLA) is designed for 8-bit, 16-bit, 32-bit and 64-bit and then compared with conventional CSLA respective architectures, this work evaluates the performance of the proposed designs in terms of delay, area, power, and their products by implementing in Xilinx fpga. This CSLA structures are implemented in booth multiplier in order to increase the efficiency of the booth multiplier.*

Index terms – Application specific integrated circuits (ASIC), area-efficient, CSLA, low power, Booth multiplier.

I. Introduction

Addition is the heart of the arithmetic unit is often the work horse of a computational circuit. They are the necessary component of a data path, e.g. in microprocessors or a signal processor. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the ext position. The major speed limitation in any adder is in the production of carries and many authors have considered the addition problem.



In rapidly growing mobile industry, faster units are not the only concern but also smaller area and less power become major concerns for design of digital circuits. In mobile electronics, reducing area and power consumption are key factors in increasing portability and battery life. Even in servers and desktop computers power dissipation is an important design constraint. Among various adders, the CSLA is intermediate regarding speed and area. In this paper we introduce Modified Carry Select-Adder (MCSLA) architecture to reduce area and power with minimum speed penalty .The MCSLA is designed by using single RCA and Binary to Excess-1 Converter (BEC) instead of using dual RCAs.

II. Function and structure of bec logic

The basic work is to use Binary to Excess-1Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. The main idea of this work is to use BEC instead of the RCA with Cin=1 in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, an n+1-bit BEC is required. A structure and the function are shown in Figure2 (a) and Table 2(a) respectively.

Figure.2(a) 4-binary to excess-1 converter

The Boolean expressions of the 4-bit BEC is

B0 = ~A0

B1 = A0^A1

B2 = A2^ (A0 & A1)

B3 = A3^ (A0 & A1 & A2)

A[3:0]	B[3:0]
0000	0001
0001	0010
.	.
.	.

Table.2(a) Function table of the 4-bit BEC

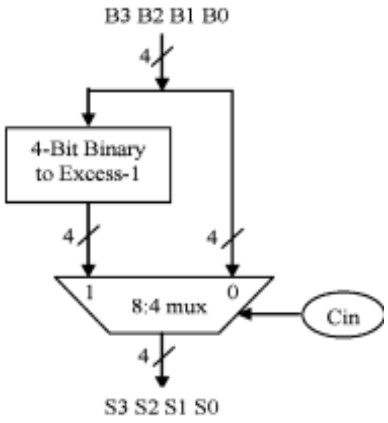


Figure.2(b) 4-b BEC with 8:4 mux.

III. Structure of conventional 16-bit mcsla

A 16-bit carry select has two types of block size namely uniform block size and variable block size. A 16-bit carry select adder with a uniform block size has the delay of four full adder delays and three MUX delays. While a 16-bit carry select adder with variable block size has the delay of two full adder delays, and four mux delays. Therefore we use 16-bit carry select adder with variable block size. Ripple-carry adders are the simplest and most compact full adders, but their performance is limited by a carry that must ripple from the least-significant to the most- significant bit. A carry-select adder achieves speeds 40% to 90% faster by performing additions in parallel and reducing the maximum carry path.

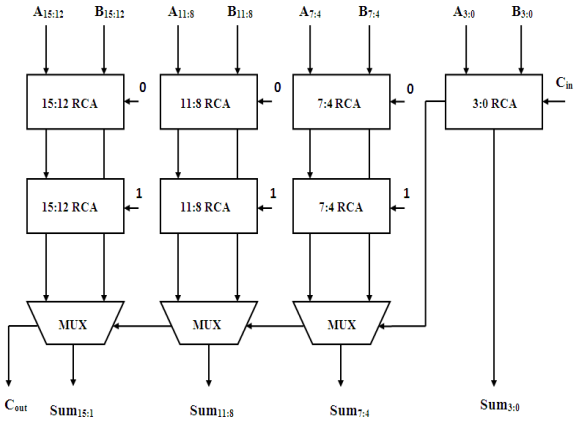


Figure.3 16-bit Conventional CSLA

A carry-select adder is divided into sectors, each of which, except for the least significant performs two additions in parallel, one assuming a carry-in of zero, the other a carry- in of one within the sector, there are two 4-bit ripple- carry adders receiving the same data inputs but different Cin. The upper adder has a carry-in of zero, the lower adder a carry-in of one. The actual Cin from the preceding sector selects one of the two adders. If the carry-in is zero, the sum and carry-out of the upper adder are selected. If the carry- in is one, the sum and carry-out of the lower adder are selected. Logically, the result is not different if a single ripple-carry adder were used. First the coding for full adder and different multiplexers of 6:3, 8:4, 10:5, and 12:6 was done. Then 2, 3, 4, 5-bit ripple carry adder was done by calling the full adder. The 64-bit Conventional CSLA was created by calling the ripple carry adders and all multiplexers based on circuit.

IV. Modified carry select adder (mcsla)

A Modified Carry Select-Adder (MCSLA) design is proposed, which make use of single RCA and Binary to Excess-1 Converter (BEC) instead of using dual RCAs to reduce area and power consumption with small speed penalty. As the base of proposed design is that the number of logic gates used in BEC is less than that of RCA. Thus BEC replaces the RCA with Cin=1 instead of using dual RCAs to reduce area and power consumption of the conventional CSLA. To replace the N-bit RCA, an N+1 bit BEC is required. The MCSLA architecture for 16-bit is shown in Figure 4.The importance of BEC logic comes from the large silicon area reduction when designing MCSLA for large number of bits.

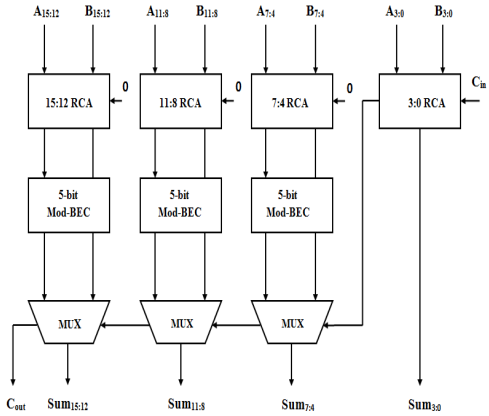


Figure.4 16-bit Modified Carry Select Adder (MCSLA)

To elaborate this, the gate calculations are made for 4-bit BEC and 4-bit RCA area as under. *For 4-bit RCA* In 4-bit RCA, four FAs are connected in a chain. Therefore the gates require to built 4-bit RCA are shown in Table 4.

AND	28
OR	16
INV	16

Table 4(a) AND, OR and INV gates in 4-bit RCA

For 4-bit BEC The 4-bit BEC can be obtained by using the Boolean equations under table 2, From these Boolean equations, the number of AND, OR and INVERT gates used to built 4-bit BEC are shown in Table 4.

AND	9
OR	3
INV	7

Table 4(b) AND, OR & INV gates in 4-bit BEC

V. Implementation in booth multiplier

The modified CSLA is implemented in a 16 × 16 bit Modified booth multiplier in order to increase the efficiency of the booth multiplier. The delay time and area of modified booth multiplier is greatly reduced when we use the modified CSLA. The structure of a modified booth multiplier is shown in fig.5. This architecture is more efficient than the conventional one in terms of area and delay. Therefore, modified Booth multiplier architecture is low area, high speed, simple and efficient for VLSI hardware implementation.

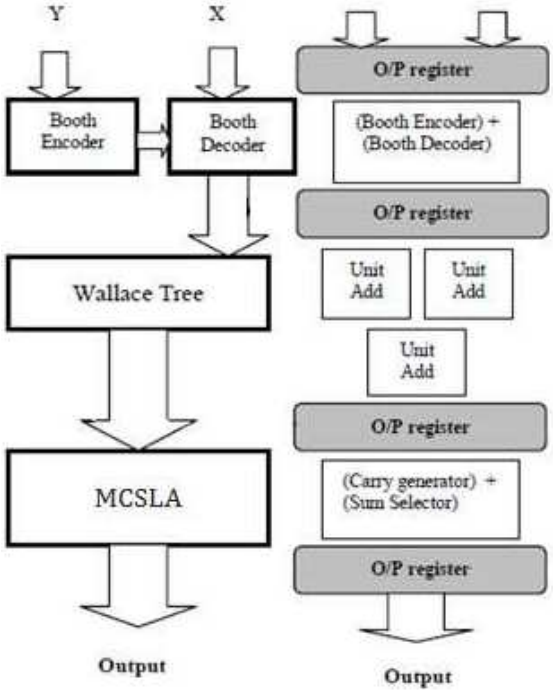


Figure.5 Booth Multiplier

VI. Implementation results

The various adders are designed using Verilog language in Xilinx ISE Navigator 13.3. And all the simulations are performed using Xilinx ISim simulator. The performance of proposed MCSLA is analyzed and compared against the conventional CSLA designs. The number of gates used in the design indicates the area of design. The power consumption is measured in terms of total power and dynamic power. The speed of the adder is estimated by the delay involved in the design. It can be seen from Table.5 that area and power consumption of MCSLA is less than that of conventional CSLA, whereas delay is more in MCSLA. This shows that area and power consumption of MCSLA is reducing at the cost of small decrease in speed. As the number of gates used in the design of MCSA are fewer than the conventional CSLA. The reduced number of gates of the MCSLA offers a great advantage in the reduction of area and total power consumption.

Design		Area (No. Of gates)	Power (in mW)	Delay (in ns)
CSLA	8-bit	543	40	9.854
	16-bit	1103	43	15.256
	32-bit	2265	46	21.950
	64-bit	4643	57	30.734
MCSLA	8-bit	378	39	11.878
	16-bit	762	41	14.796
	32-bit	1548	43	21.720
	64-bit	3174	50	31.892

Table.6 Comparison of area, power and speed of Conventional and Modified CSLA

Word-size of Adder	Area Reduction (in Percent)	Power Consumption reduction (in percent)	Delay Overhead (in percent)
8-bit	16.5	8	15
16-bit	20.62	14	9
32-bit	22.21	16	6.9
64-bit	22.92	17	4

Table.6.1 Reduction Percentage of Area, Power And Speed of Modified CSLA

Logic Utilization	Conventional Booth multiplier	Modified Booth multiplier	% Reduction
Number Of Slices	394	377	4.3
Number of LUT'S	749	718	4.1
Delay calculation	51.92ns	22.38ns	56.8

Table.6.2 Comparison of Conventional and Modified Booth Multiplier

VII. Conclusion

In this paper, a Modified Carry Select-Adder (MCSLA) is designed by using single Ripple Carry Adders (RCA) and Binary to Excess-1 Converter (BEC) instead of using dual RCAs to reduce area and power consumption with small speed penalty. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power. The MCSLA architecture for 8-bit, 16-bit, 32-bit and 64-bit is designed and then compared with conventional CSA respective architectures. MCSLA shows reduction in area and power consumption in comparison with conventional CSLA with small increase in delay. The MCLA is implemented in modified booth multiplier which reduces the number of slices, LUT's and delay by 4.3%, 4.1% and 56.8% respectively. The synthesis is done by using Xilinx ISE.

VIII. References

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