An Improved Configuration of Cascaded H-Bridge for Level Doubling

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Abstract

In this paper a level circuit is introduced for recently proposed new cascaded H-Bridge multilevel inverter topology. With the proposed modifications output level can be doubled with reduced switch count, driver circuits and diodes. The proposed circuitry requires less number of semiconductor switches, driver circuits, diodes as compared to existing recently proposed cascaded H-Bridge topology. The performance and functional accuracy of the proposed topology in generating all voltage levels for an 11-level inverter are validated by simulation in MATLAB/SIMULINK environment.

Keywords: Cascaded Multilevel Inverter, Multilevel Inverter, Voltage Source Inverter, Level Doubling

INTRODUCTION

Nowadays multilevel inverter is gaining more popularity for industry and academia field as compared to two level inverter due to its high quality output waveform. The advantages of multilevel inverter over two level inverter are: high power quality, lower order harmonics, lower switching losses, and better electromagnetic interference [1], [2]. The basic type of multilevel inverters is: neutral point clamped (NPC) multilevel inverter used in motor drive application [3], flying capacitor (FC) multilevel inverter used in medium voltage application [4]-[5] and cascaded H-Bridge (CHB) multilevel inverter specially suited for renewable energy systems or static VAR compensators [6]. The generated output level of multilevel inverter depends on circuitry devices. Hence, with the increment of output levels the device count increases and impose more complexity and cost on the system. The NPC requires large number of diodes, FC requires bulky capacitor and in case of CHB linearly switching devices increases with the increasing output voltage levels.

Other than the basic multilevel inverter, some approaches are suggested to achieve more output levels without increasing the device count in recent years. One of the such topology is the multilevel dc link inverter proposed in [7]-[8]. This topology is highly modular and simple. However, the topology does not consider reduction in the number of components used. In [9] a new topology is proposed which is simple and requires non isolated dc sources but the main disadvantage of this structure is related to its bidirectional power switches, which cause an increase in the number of IGBTs and the total cost of the inverter. The topology presented in [10] considers reduction in the components. The topology is basically based on symmetric topology hence the used dc voltage sources have same values. However, the number of switching devices still remains high in these topologies.

The so-called Cascaded H-Bridge multilevel inverter based on developed H-Bridge has been recently proposed in [11] with a view to reduced the device count. The topology is so called because it is obtained by adding two unidirectional power switches and one dc voltage source to the H-bridge inverter structure. It is shown in [11] that the Cascaded H-Bridge multilevel inverter leads to a substantial decrease in component count as compared to the classical topologies. It also leads to simplicity and better efficiency.

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In this paper, a level doubling circuit has been added to the recently proposed cascaded H-Bridge topology in such a fashion so as to double the output levels. Circuitry and working of the proposed topology is presented and discussed. Also, in continue a comparison between proposed topology, and a recently developed topology is carried out. Finally, in order to verify the proposed topology, implementation is carried out for single phase 11-level inverter in MATLAB/SIMULINK environment.

CASCADED H-BRIDGE AND ITS IMPROVED DESIGN

A five-level inverter based on Cascaded H- Bridge topology is shown in Fig.1. It consists of six power switches and two sources V_{dc1} and V_{dc2} such that $V_{dc1} = V_{dc2}$

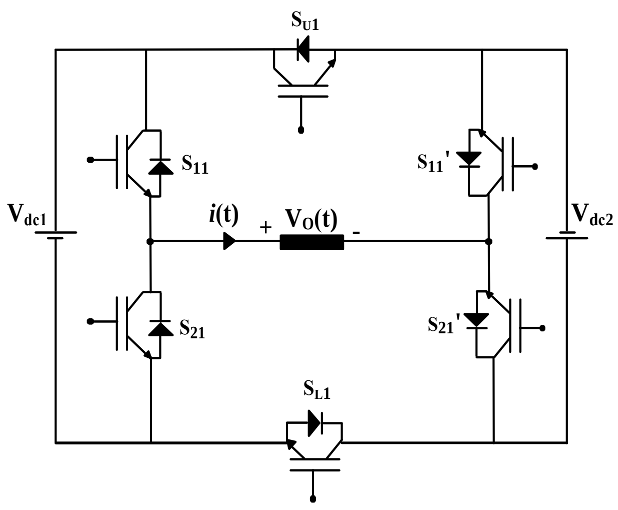

Fig. 1. A five-Level Cascaded H-Bridge as Proposed in [11]

The Cascaded H-Bridge topology with the proposed improved voltage doubling design is shown in Fig.2. The structure consists of eight switches in which six switches are forward conducting-unidirectional-blocking and two added switches are bidirectional-conducting-bidirectional-blocking along with four dc sources. Sources V_{dc3} and V_{dc4} and switches S_A and S_B are added in Fig.1. for doubling the output levels of cascaded H-Bridge topology. Increasing of output voltage levels with reduced number of total component count increases the system reliability, reduces system cost, size and required installation area. The voltage sources are selected in such a fashion that to the original network are $V_{dc1} = V_{dc2} = V$ and $V_{dc3} = V_{dc4} = V/2$. The working states of the proposed structure are shown in Table I. It can be seen that eleven levels are obtained with the proposed structure in the output waveform, these levels are 0, $\pm V/2$, $\pm V$, $\pm 3V/2$, $\pm 2V$ and $\pm 5V/2$. In Table I. the on state of corresponding switch is represented by 1 whereas 0 indicates the off state.

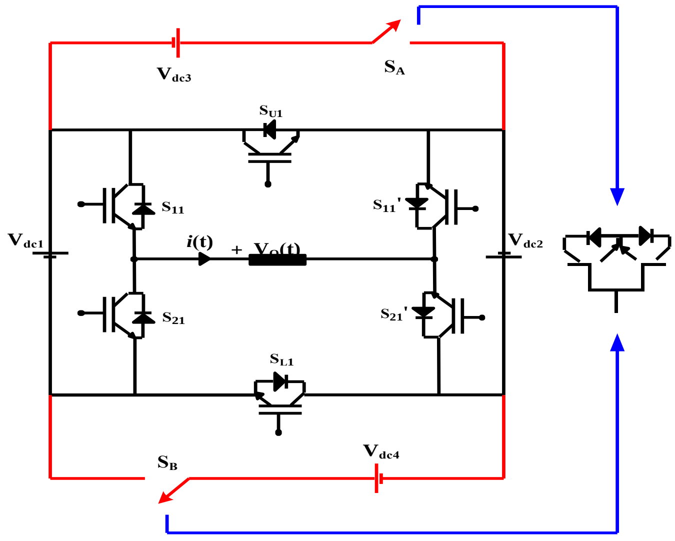

Fig. 2. Proposed Multilevel Inverter for Level Doubling

COMPARISON OF THE PROPOSED TOPOLOGY WITH CLASSICAL AND RECENTLY PROPOSED CASCADED H-BRIDGE TOPOLOGY

The eleven-level structure based on the combination of recently proposed Cascaded H-Bridge multilevel inverter with level doubling circuit consists of four sources and eight power switches. An eleven level recently proposed Cascaded H-Bridge multilevel inverter proposed in [11] would require five sources and twelve semiconductor switches. Thus, the proposed structure leads to a requirement of lesser number of components as compared to the original Cascaded H-Bridge multilevel inverter topology.

A general comparison of the proposed circuitry with the classical cascaded H-Bridge multilevel inverter and recently proposed Cascaded H-Bridge topology in [11] is shown in Table II for a single phase configuration.

Table I. Output Voltages for States of Switches

STAT E NUM BER	SWITCHES STATE								OUTP UT VOLT AGE
	S_{11}	S_{11}’	S_{21}	S_{21}’	S_{U1}	S_{L1}	S_A	S_B	
1	1	1	0	0	1	0	0	0	0
2	0	0	1	1	0	1	0	0	0
3	0	0	1	1	0	0	0	1	V/2
4	1	0	0	1	0	1	0	0	V
5	0	1	1	0	0	0	0	1	3V/2
6	1	1	0	0	0	1	0	0	2V
7	1	1	0	0	0	0	0	1	5V/2
8	1	1	0	0	0	0	1	0	-V/2
9	1	0	0	1	1	0	0	0	-V
10	0	1	1	0	0	0	1	0	-3V/2
11	0	0	1	1	1	0	0	0	-2V
12	0	0	1	1	0	0	1	0	-5V/2

Requirement of various components for the topology proposed in this paper and the so-called classical and recently proposed Cascaded H-Bridge topology is shown in Table II. for single phase configuration. It is important to note that individual switches, diodes, driver circuit and total components required are less in the proposed structure as compared to cascaded H-Bridge structure.

When requirement of power switches for eleven-level voltage waveform is considered, the proposed topology require only 8 power switches diodes and drivers whereas the classical and recently proposed Cascaded H-Bridge topologies require 16 and 12 switches, diodes and drivers respectively. It can also be observed from Table II that with the reduction of total component count in the proposed topology for higher voltage level the cost of the system, its size and required area is also reduced. Another important parameter related with switches is the loss incurred is also reduces with reduction of switches.

SIMULATION RESULTS

In order to validate the functionality of the proposed structure, a simulation study is carried out using MATLAB/Simulink software package. The circuit shown in Fig.2 is modelled with $V_{dc1} = V_{dc2} = V = 50$V and $V_{dc3} = V_{dc4} = V_{dc}/2 = 25$V. Here simulation is done for *R and R-L* load both. *R* load is considered at the output terminals with $R = 2\Omega$. An *RL* load is considered at the output terminals with $R = 2\Omega$ and $L = 5$ mH. Since the structure is an eleven level inverter, a sine-triangle pulse width modulation (PWM) is administered with ten carrier signals of sinusoidal reference signal of 50 Hz frequency.

Table II. Comparison Between Topologies

Multilevel inverter components	Classical cascaded H- Bridge	Topology proposed in [11]	Proposed structure
IGBT switches	2(n-3)	n+1	2(n+1)/3
Diodes	2(n-3)	n+1	2(n+1)/3
Driver circuit	2(n-3)	n+1	2(n+1)/3
Total component count	6(n-2)	3(n+1)	2(n+1)

‘n’ is output voltage level

The obtained load voltage and current waveforms for *R* load with their corresponding harmonic spectrum are shown in Figs. 3-6 and for *RL* load the voltage and current waveforms with their corresponding harmonic spectrum are shown in Figs. 7-10. The output voltage waveform for *R* load has total harmonic distortion (THD) of 11.28% with third and fifth harmonics being 0.06% and 0.13%, respectively. Also, the THD of load current is observed to be same as voltage THD.

The output voltage waveform for *RL* load has total harmonic distortion (THD) of 11.30% with third and fifth harmonics being 0.06% and 0.14%, respectively. Also, the THD of load current is observed to be less than 1% for the aforesaid inductive load.

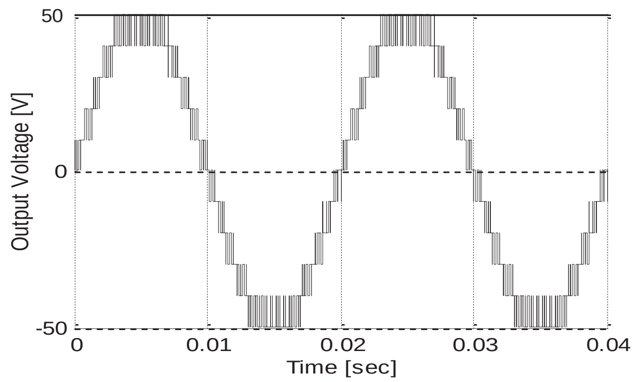

Fig. 3. Simulation results of the 11-level output voltage for R-load

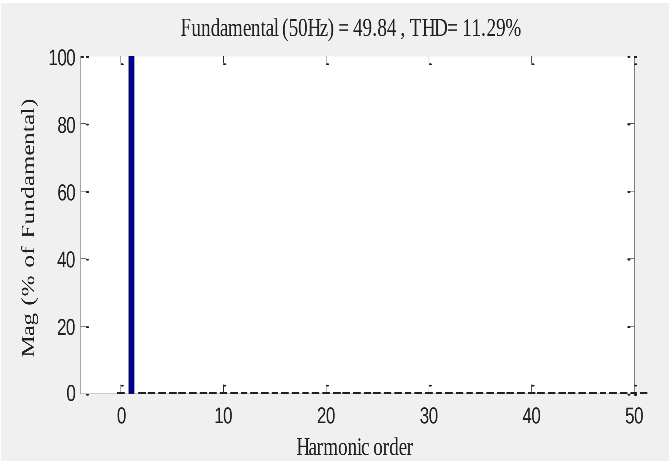

Fig. 4. Harmonic spectrum of 11-level output voltage for R-load

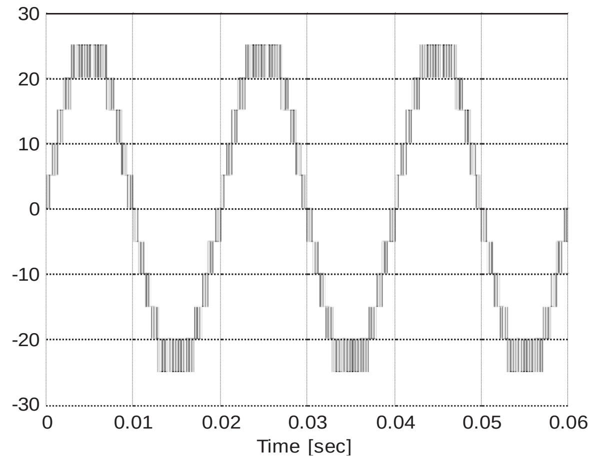

Fig. 5. Simulation results of the 11-level load current for R- load

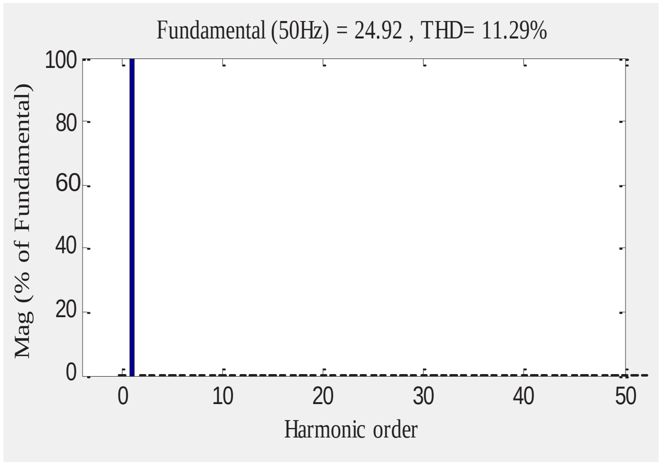

Fig. 6. Harmonic spectrum of 11-level load current for R-load

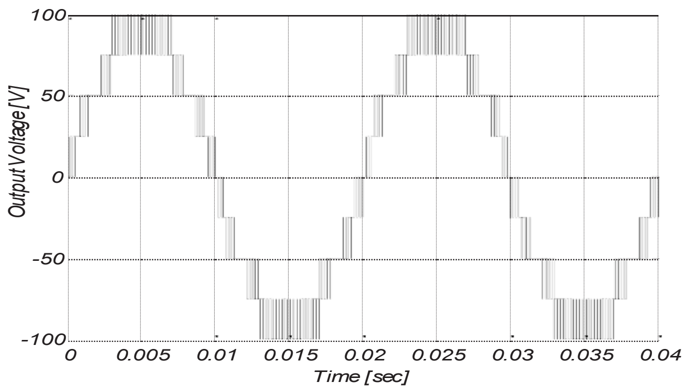

Fig. 7. Simulation results of the 11-level output voltage RL-load

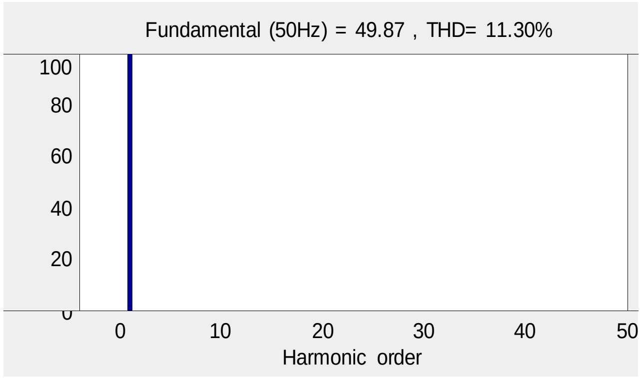

Fig. 8. Harmonic spectrum of 11-level output voltage for RL- load

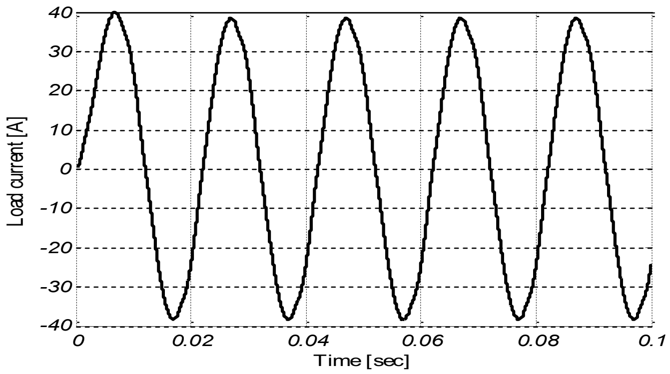

Fig. 9. Simulation results of the 11-level load current RL-load

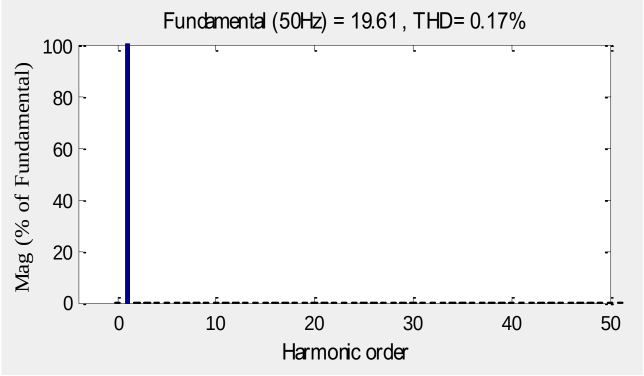

Fig. 10. Harmonic spectrum of 11-level load current

In Table III the total harmonic distortion (THD) and harmonic orders content of voltage and current for *R* and *RL* load is shown. With the simulation plot it is clearly visible that voltage THD of the load i.e, *R* and *RL* load is approximately same. In Case of current THD, the *RL* load current having very low THD as compared to *R* load current because inductor (L) acts as filter for current.

Table III. Harmonic Analysi for R and Rl Load

Harmonic order and THD (in %)	*R load*	*RL load*
Voltage THD	11.29	11.30
Current THD	11.29	0.17
3rd	0.06	0.06
5th	0.13	0.14
7th	0.22	0.22
9th	0.03	0.13
11th	0.01	0.01
13th	0.08	0.08
15th	0.03	0.03
17th	0.13	0.13
19th	0.09	0.09
21th	0.08	0.08

CONCLUSION

In this paper a recently proposed Cascaded H-Bridge topology is modified for doubling output voltage level so as to reduce the total number of components. A comparison of the Cascaded H-Bridge shows that a structure with voltage level doubling requires much lesser number of components (DC sources as well as power switches). Working of the structure is shown with the help of an eleven-level inverter. Simulation results based on MATLAB/Simulink are presented to validate the proposed concept.

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