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A Low Power DBI Based CRC Design Using GDI Technology

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Abstract: In this paper, we implemented the data bus inversion cyclic redundancy check using Gate Diffusion input technique. Initially to reduce signaling power in the single-ended interface Data Bus Inversion (DBI) is required, in which the state of the data to be transmitted may or may not be inverted prior to transmission. a new CRC methodology which is based on the DBI is to reduce the CRC calculation delay time and area overhead for high-speed memory devices. GDI logic is introduced as an alternative to CMOS logic. It is a low power design technique which offers the implementation of the logic function with fewer numbers of transistors. GDI gates provide reduced voltage swing at their outputs. In GDI based CRC no of transistors are reduced and power consumption and area is decreased.

Keywords: Cyclick redundency check, Data bus inversion, Gate diffusion input.

I. Introduction

In DBI transmitted data may or may not inverted depends up on encoding algorithm, prior to transmission. The DBI consists of full adder and from this we can extract the information related to the even number of data. To reduce the SSO (Simultaneous Switching Output) noise and improve the signal integrity for the high speed data rate communication system. Cyclic redundancy check code is very useful for detecting and correcting the errors in the signals or data. A low power high speed CRC's plays a vital role in Communication systems [1]. To get computer system process speed, valid data window is required and it is a crucial part for reliable data transmission and also it is the main reason to cause error between semiconductor memory device and computer system. If any device uses low electrical power, its importance increases very rapidly. The semiconductors such as DDR4 SDRAM (Double Data Rate 4 Synchronous Dynamic Random Access Memory) and GDDR5 (Graphic DDR5) required very high speed data rate and low power, CRC (Cyclic Redundancy Check) is required [2,3].

Moreover, the difficulty becomes worse in the low power memory device [2,4]. The DBI based CRC reduces the CRC calculation delay time and area overhead for high speed memory devices, and the DBI data can be utilized to detect the data bit errors [5]. This method used for high speed memory devices and quantitatively analyzes the improvements and the errors detection.

The basic GDI cell is shown in Fig. 1 though it looks similar to conventional CMOS inverter the source / drain diffusion input of both PMOS and NMOS transistor is different. In conventional inverter circuit, source and drain diffusion input of PMOS and NMOS transistors are always tied at VDD and GND potential, respectively. The diffusion terminal of conventional CMOS inverter acts as an external input in the GDI cell. It helps in the realization of various Boolean functions such as AND, OR, MUX, INVERTER. In this work DBI based CRC is implemented for low power and small area applications.

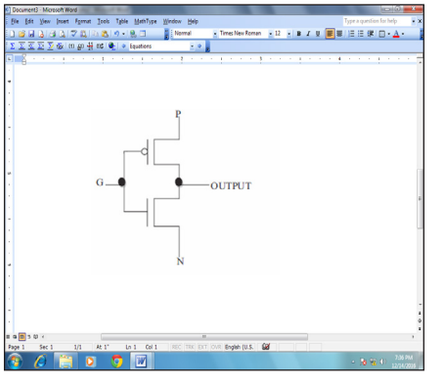

Fig. 1: Basic GDI Cell

Table I: Different Logic Function Realization Using GDI Cell

N	P	G	OUT	Function
0	B	A	ÃB	F1
B	1	A	Ã+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	ÃB+AC	MUX
0	1	A	Ã	NOT

II. Full Swing XOR Gate

The main drawback GDI cell is low swing, to provide full swing at the output the proposed XOR gate is designed using 4 transistors (excluding the inverter for complementary input signal). The schematic of XOR gate using GDI logic with full swing is shown in Fig.

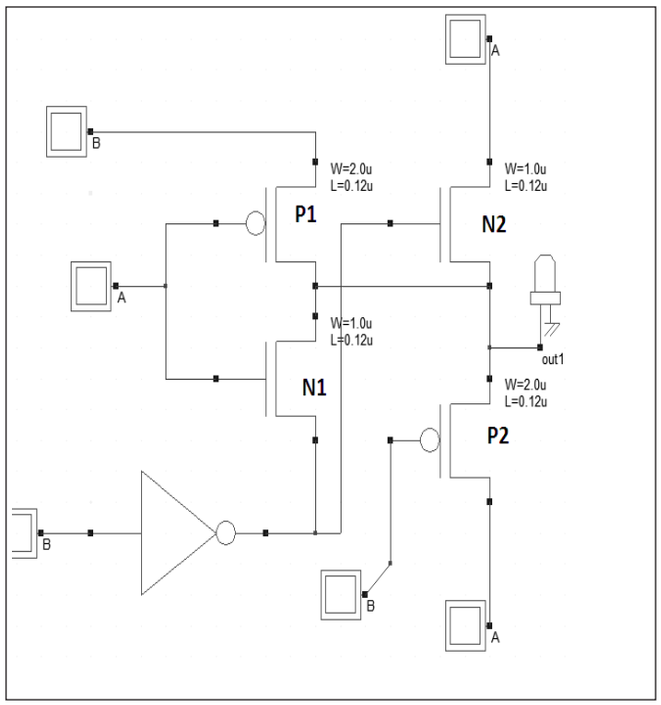

Fig. 2: Full Swing XOR Gate

The operation of proposed XOR gate is explained as follows: The existing design lacks in full swing operation for two cases when AB = 00 and 10. The techniques presented in the literature directly use supply rail VDD for strong '1' and VSS for strong '0'. But the proposed design does not use supply rails either GND or VDD for obtaining the perfect output. It uses input, but only with proper biasing of a necessary transistor, which may be either PMOS or NMOS. This in turn would depend on the input level, to mitigate the threshold voltage loss, which occurs in conventional XOR design.

For AB = 00, transistor P1 (PMOS), P3 (NMOS) and P4 (PMOS) conduct. The P3 transistor is responsible for delivering strong '0'. Likewise, another case when AB = 10, transistor P2 (NMOS), P3 (NMOS) and P4 (PMOS) work for the given input, in which P4 passes strong '1' to the output. Whereas in other cases, namely AB = 01 and 11, the transistors P3 and P4 do not change the output potential. Hence, the correct output for XOR gate is attained.

III. Proposed GDI Based DBI-CRC

The DBI consists of full adder and from this we can extract the information related to the even number of data. To reduce the SSO (Simultaneous Switching Output) noise and improve the signal integrity for the high speed data rate communication system, DBI features has been used.

If more than four bits of a byte lane are Low then DBI invert output data. Hence, DBI enables fewer bits switching, which results in less noise and a better data eye. Moreover, we can extract the number of double and sextuple (6 bit) of '1' bits from the DBI feature. And also it can extract the position of double 1's and sextuple 1's. This information is applied to the conventional CRC to improve double bits error detection coverage. Conventional DBI based CRC scheme is shown in the Fig. 3.

When data write to the memory, DB_s signal will send from system to memory and then check the data error between DB_s and DB_m. Simultaneously, calculate the CRC syndrome polynomial S0~S7 in the memory. Finally, the odd data error can be detected by comparing the system data CRC_s and CRC_m. CRC_s is the system data, which is send to the memory and CRC_m is the generated data in the memory which is based on the DQ data in the memory. Also, the partial even data error can be detected by comparing the system data DB_s/DBI_s and DB_m/DBI_m. Fig. 2 shows the conventional CRC configuration.

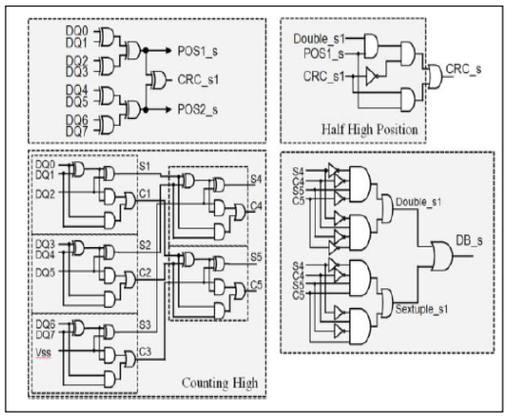

Fig. 3: Conventional CRC Scheme

The expression (1) shows the whole error detection components.

E1 = DBI_s XOR DBI_m,
E2 = DB_s XOR DB_m,
E3 = CRC_s XOR CRC_m
Therefore Error = E1 + E2 + E3 (1)

Conventional DBI based CRC bit mapping configuration needs to change from the DDR4 data configuration.

IV. Proposed GDI Based DBI-CRC Scheme

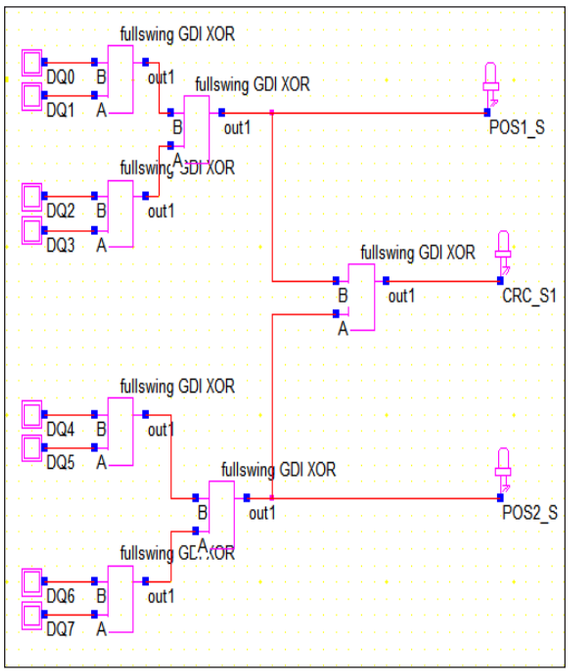

Fig. 4: GDI CRC Generator

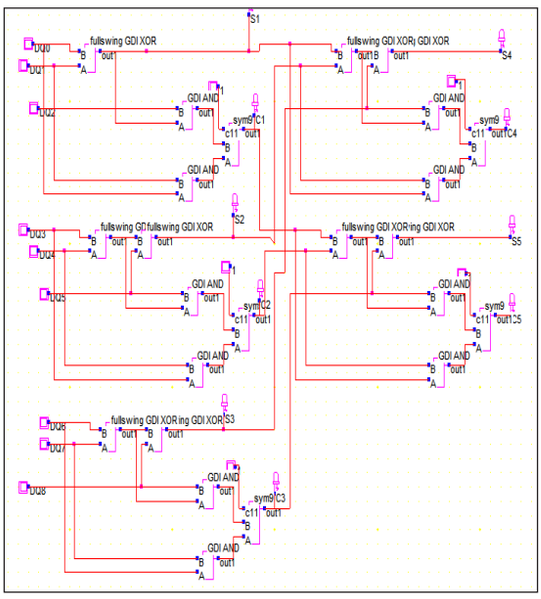

Fig. 5: GDI CRC Count High

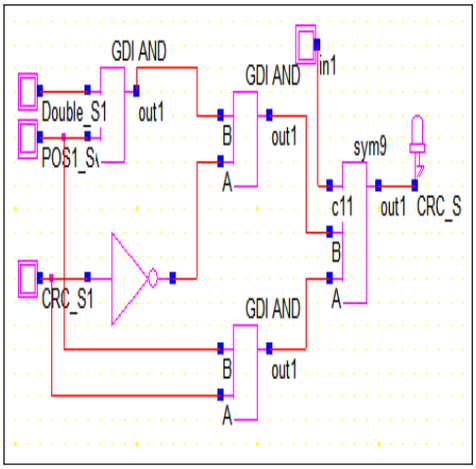

Fig. 6: Half High Position

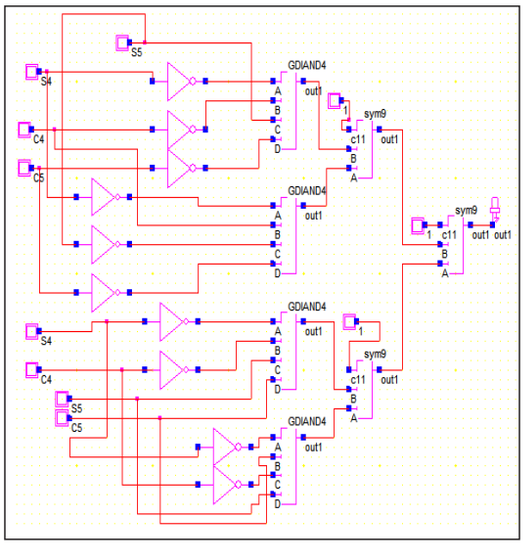

Fig. 7: Error Detector

V. Simulation Results

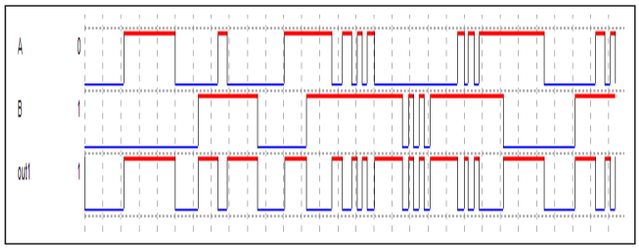

Fig. 8: Full Swing XOR Gate Using GDI Logic

In an existing design the output swing is poor when inputs AB = 00 and 01, but using full swing GDI output swing is HIGH for all four inputs.

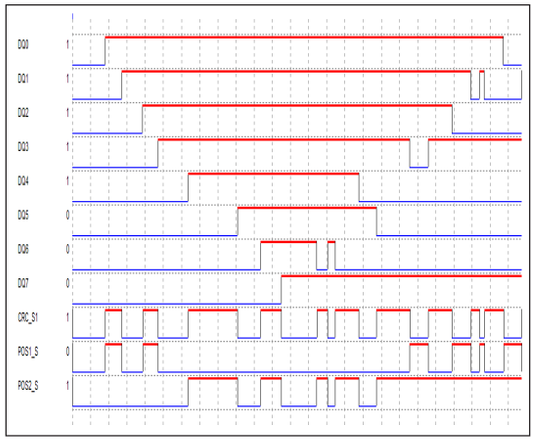

Fig. 9: CRC Generator

The Fig. 9 shows the CRC generator output. We have taken DQ0 - DQ7 (8 bit data) as input data and we obtained three outputs namely POS1_S (Position 1), CRC_S1 (CRC Code) and POS2_S (Position 2).

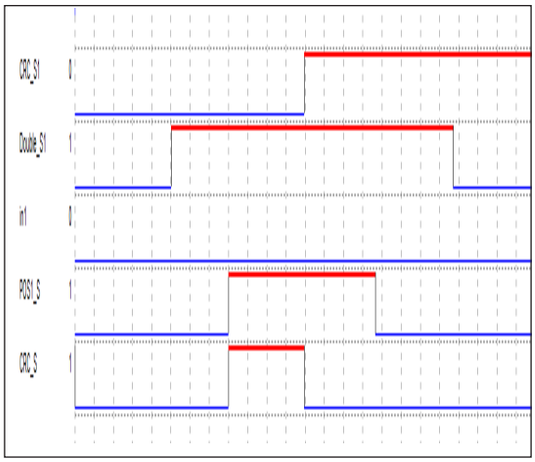

Fig. 10: Half High Position

The Fig. 10 shows the Half High Position output. We have taken CRC_S1 (CRC Code), POS1_S (Position 1), DOUBLE_S1 (Double error detection) and IN1 as inputs and we observed that CRC_S is fixed.

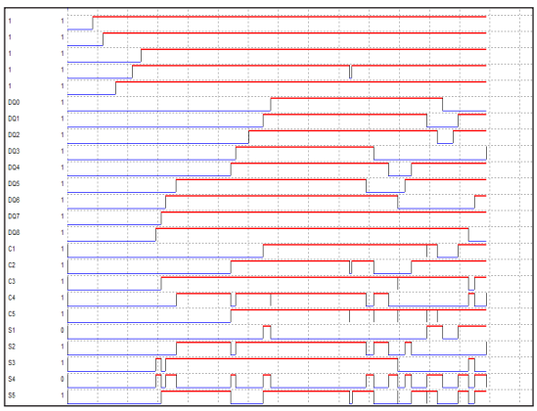

Fig. 11: Counting High

The Fig. 11 shows the Counting High output. We have taken DQ0 - DQ7 (8 bit data) as input data and we obtained outputs namely S1-S5, C1-C5 and HIGH.

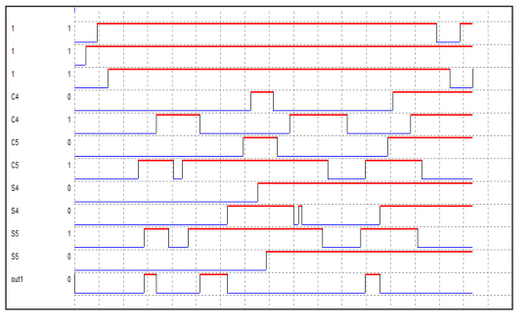

Fig. 12: Error Detector

The Fig. 12 shows the Error Detector output. We have taken S4, S5, C4, C5 as inputs and we obtained output namely out1 (DB_S).

VI. Conclusion

All blocks in the CRC scheme are implemented using GDI technology. The proposed DBI based CRC using GDI technology is taking less no of transistors and area where compare to conventional DBI based CRC.

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